Link Street® 88E6350R/88E6350/88E6351

7 Port AVB Gigabit Ethernet Switch with 5 Integrated PHYs and Synchronous Ethernet

Datasheet Part 1 of 3: Overview, Pinout, Applications, Mechanical and Electrical Specifications

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	**Note:** Provides related information or information of special importance.
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Preface

About this Document

The 88E6350R/88E6350/88E6351 datasheet is a three-part set that includes the following documents:

- **88E6350R/88E6350/88E6351 Datasheet Part 1: Overview, Pinout, Applications, Mechanical and Electrical Specifications**

  Provides a feature list and overview describing the 88E6350R/88E6350/88E6351. It also provides the pin description, pin map, mechanical drawings, and electrical specifications.

- **88E6350R/88E6350/88E6351 Datasheet Part 2: Switch Core**

  Provides a description of the switch core of the 88E6350R/88E6350/88E6351 and related register tables.

- **88E6350R/88E6350/88E6351 Datasheet Part 3: Gigabit PHYs**

  Provides a description of the Gigabit PHYs of the 88E6350R/88E6350/88E6351 and related register tables.

Table 1 shows the 88E6350R/88E6350/88E6351 devices feature differences.

Table 1: 88E6350R/88E6350/88E6351 Device Feature Differences

		88E6350R	88E6350	88E6351
Features	GE Switch Ports	7	7	7
	# GE PHYs	5	5	5
	RGMII/MII	2	2	2
	# GMII/MII (Shared w/RGMII)	0	2 (Indicated by BLUE font in Figure 1)	2
	Jumbo Frame Support	10K bytes	10K bytes	10K bytes
	Packet Buffer Memory	1 Mbit	1 Mbit	1 Mbit
	# MAC Addresses	1K	1K	8K
AVB	802.1AS/Qat/Qav/1588	Yes	Yes	Yes
	Timing Application Interface (TAI)	No	Yes	Yes
	Synchronous Ethernet	No	No	Yes
QoS	Queues per Port	4	4	4
	802.1p, Port, TOS/DS, IPv6, TC, MAC	Yes	Yes	Yes
	Programmable QoS Weighting	No	No	Yes
VLAN	Port -based VLANs	Yes	Yes	Yes
	802.1Q VLANs	64	64	4096
	Double Tagging (Q in Q)	Yes	Yes	Yes
Management	Remote Management/Ethertype DSA	Yes	Yes	Yes
	Layer 2 Policy Control Lists (PCL)	No	No	Yes
	802.1D/w/s Spanning Tree	Yes	Yes	Yes
	Port Mirroring/Port Trunking	Yes	Yes	Yes
	IPv4 IGMP & IPv6 MLD Snooping	Yes	Yes	Yes
Other	Ingress Rate Limiting Resources	2/port	5/port	5/port
	Egress Rate Shaping	Enhanced	Enhanced	Enhanced
	802.1X Port and MAC-based Authentication	Yes	Yes	Yes
	GPIO Pins	2	7	7
	Package	128-pin TQFP	176-pin LQFP	176-pin LQFP
	Industrial grade	Yes	No	Yes

Figure 1 shows the overall block diagram for the 88E6350R/88E6350 devices.

Figure 1: 88E6350R/88E6350 Block Diagram

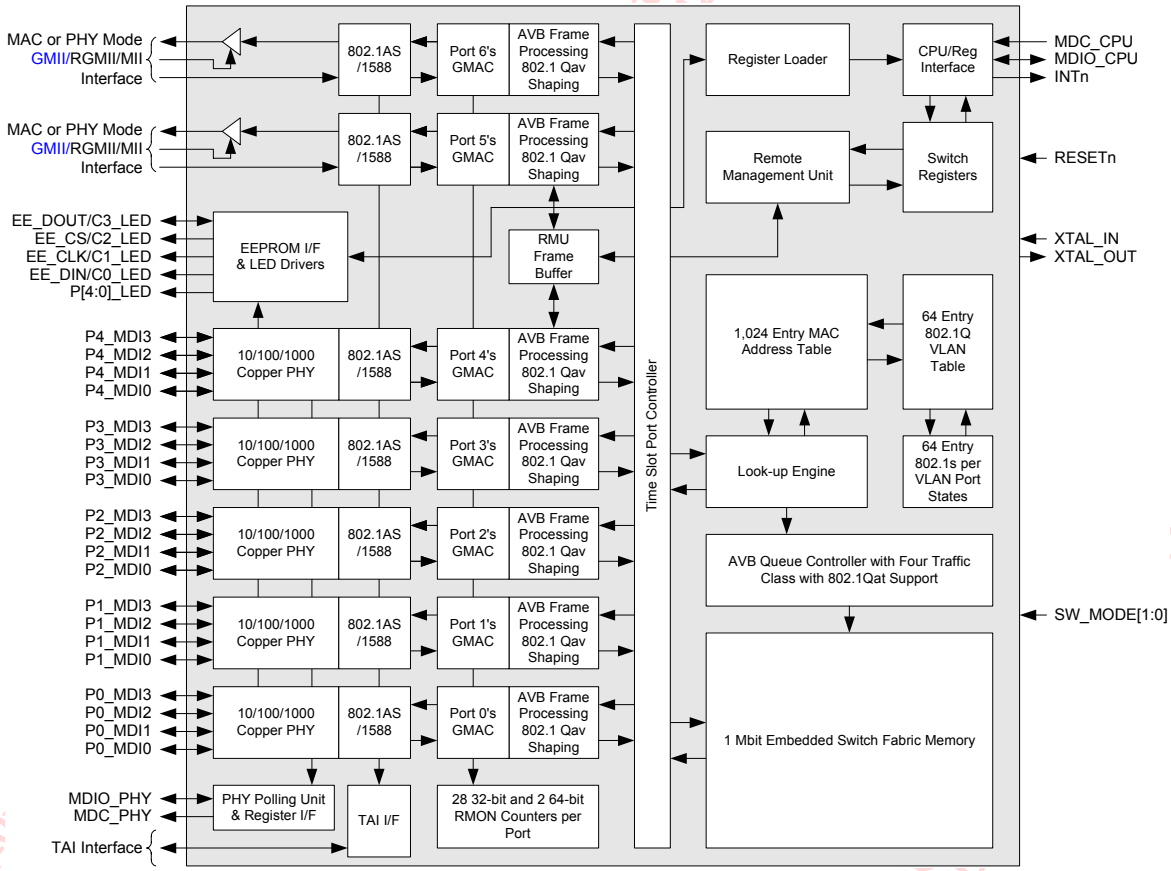
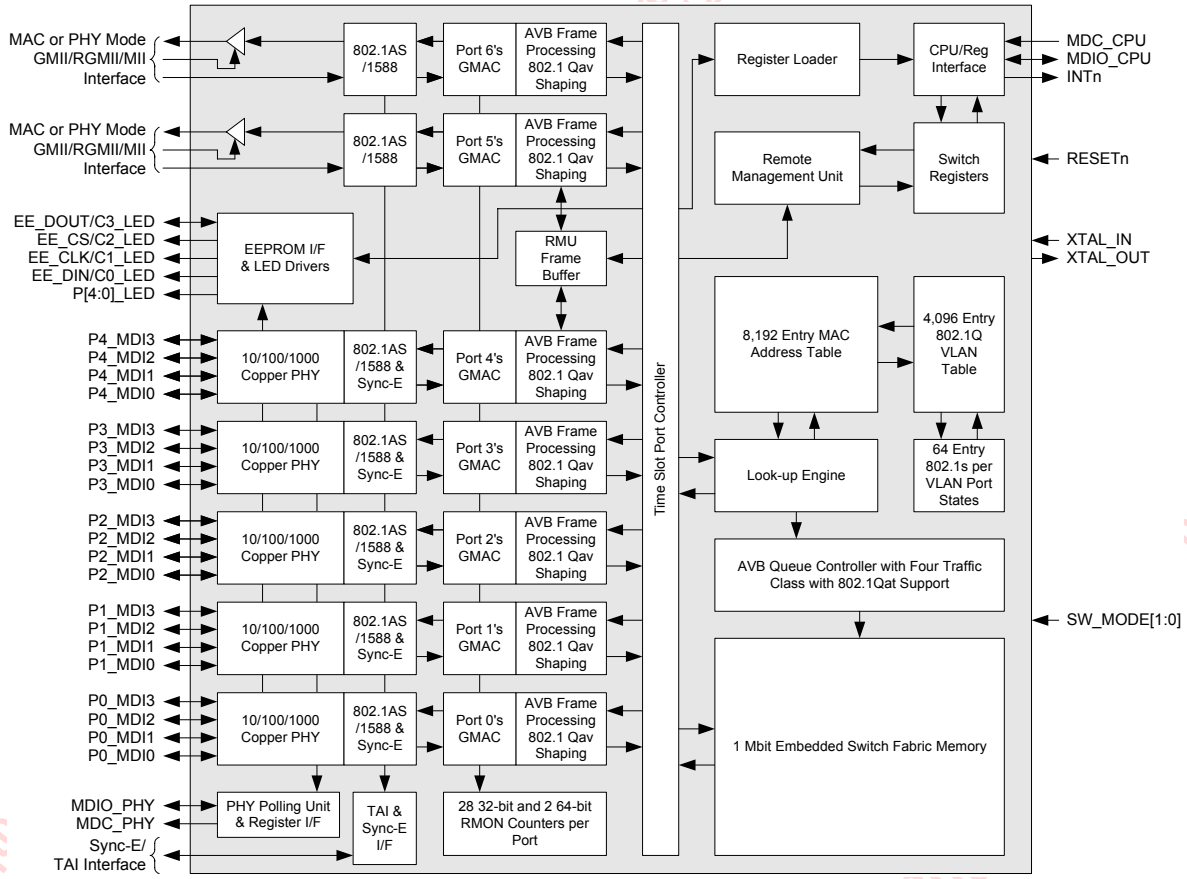


Figure 2 shows the overall block diagram for the 88E6351 device.

Figure 2: 88E6351 Block Diagram



Link Street®
88E6350R/88E6350/88E6351
7 Port AVB Gigabit Ethernet Switch with 5 Integrated PHYs and Synchronous Ethernet

OVERVIEW

The Marvell® 88E6350R/88E6350/88E6351 device is a single-chip 7-port Gigabit Ethernet switch with five integrated Gigabit Ethernet transceivers supporting the latest IEEE 802.1 Audio Video Bridging (AVB) standards. The device uses these AVB technologies to identify and reserve network resources for AVB traffic streams and supports precise isochronous streaming capability. These AVB protocols enable timing sensitive multimedia streams (such as digital video, audio, or industrial control traffic) to be sent over an Ethernet network with low latency and robust Quality of Service guarantees.

The 88E6351 device also supports Synchronous Ethernet.

This device contains five 10/100/1000 triple speed Ethernet transceivers (PHYs), and two digital interfaces. The 88E6350R device offers two RGMII/MII ports in a 128-pin TQFP package, while the 88E6350 device offers two full GMII/RGMII/MII ports in a 176-pin TQFP package. The 88E6350R/88E6350/88E6351 device is designed to work in all environments. True Plug-and-Play is supported with Auto-Crossover, Auto-Negotiation, and Auto-Polarity in the PHYs, along with bridge loop prevention (using Port States).

The device contains seven independent 802.3 media access controllers (MACs) supporting up to 10K byte JUMBO frames, a high-speed, non-blocking four traffic class QoS switch fabric that uses the unique Marvell Dynamic Queue Limit architecture. The QoS architecture switches packets into one of four traffic class queues based upon Port, IEEE 802.1p, IPv4 Type of Service (TOS) or Differentiated Services (Diff-Serv), IPv6 Traffic Class, 802.1Q VLAN ID, DA MAC address or SA MAC address. The device also contains a high-performance address lookup engine with support for up to 1K active nodes, and a 1 Mbit frame buffer memory. Back-pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The MAC units in the devices comply fully with the applicable sections of IEEE 802.3.

The sixth and seventh ports' RGMII/GMII interfaces support a direct connection to Management or Router CPUs with integrated MACs. These interfaces, along with BPDU handling for IEEE 802.1D Spanning Tree Protocol, 802.1w Rapid Spanning Tree, 802.1s Multiple VLAN Spanning Tree, programmable per-port VLAN configurations, 802.1Q and Port States, support fully managed switches and truly isolated WAN vs. LAN firewall applications. The device supports 64 802.1Q VLAN IDs which can be enabled on a per port basis. Three levels of 802.1Q security is supported with error frame trapping and logging.

The device supports multiple address databases (up to 64), which allows packet routing without modification of the MAC address. This allows the same MAC address to exist multiple times in the MAC Address database with multiple port mappings, to completely isolate the WAN from the LAN database.

The PHYs in the device are designed with the Marvell® cutting-edge mixed-signal processing technology for digital implementation of adaptive equalization and clock data recovery. The device integrates MDI interface termination resistors into the PHYs. The integrated resistors facilitate easier board layout and reduces board cost by reducing the board's size and the number of external components. Special power management techniques are used to facilitate low power dissipation and high port count integration. Both the PHY and MAC units in the devices comply fully with the applicable sections of IEEE 802.3, IEEE 802.3u, and IEEE 802.3x standards.

The PHYs also include an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

Up to 20 LEDs can be directly driven by the device, which supports both single and dual color LEDs. The combining of multiple ports Link/Activity LED into a single LED is also supported.

The device's many operating modes can be configured using SMI (serial management interface - MDC/MDIO) or through in-band management via an Ethernet frame. The device also supports a standalone QoS mode or configuration via a low cost serial EEPROM.

The device is designed for cost-sensitive Gigabit Ethernet switch systems that require Quality of Service, Trunking, Stacking, and/or Spanning Tree.

Highlighted Features

- Supports 802.1 Audio Video Bridging Standards
  - 802.1AS - Precise Timing Protocol
  - 802.1Qat - Stream Reservation Protocol
  - 802.1Qav - Egress Pacing and Shaping
- Supports 1588v2 over Layer 2 and Layer 4
- Timing Application Interface for AVB end nodes (88E6350/88E6351 only)
- Synchronous Ethernet support (88E6351 only)
- Supports up to 10K Byte Jumbo frames
- 'Best-in-Class' per port TCP/IP Ingress Rate Limiting along with independent Storm Prevention
- 2 (88E6350 device) or 5 (88E6351 device) Ingress Rate Limiting buckets per port, supporting Rate-based and Priority-based rate limiting
- Non-Rate Limited frames based on SA or DA
- Remote Management capabilities allow device configuration and readback via Ethernet frames
- Per port, programmable MAC hardware address learn limiting
- Quality of Service support with four traffic classes
- QoS determined by Port, IEEE 802.1p tagged frames, IPv4's Type of Service (TOS) & Differentiated Services (DS), IPv6's Traffic Class 802.1Q VID, Destination MAC address, or Source MAC address
- Frame priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- Queue priority overrides based on DA, SA, VID, Ethertype, BC, IP, PPPoE, ARP, or Snoop
- Strict, Weighted, or mixed mode QoS selectable per port
- 802.1Q VLAN support
- Supports multiple provider ports within a single chip via a programmable Ethertype per port
- Enhanced 802.1s Per VLAN Spanning Tree supporting up to 64 spanning tree instances
- Integrated MDI interface termination resistors
- Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature
- Single and Dual color LED support
- Single Link/Activity LED programmable across multiple ports
- Programmable QoS weighting (88E6351 device only)
- Layer 2 Policy Control Lists (PCL) (88E6351 device only)

Features

- Marvell® Header for increased Routing performance
- Shared 1 Mbit on-chip memory-based switch fabric with true non-blocking switching performance
- High performance lookup engine with support for up to 1K/8K MAC address entries with automatic learning and aging
- Supports the Marvell Distributed Switching Architecture (DSA) for STP, up to 32 cascaded devices, and CPU-directed packet processing
- MAC SA based 802.1X authentication
- Port Trunking and Port Monitoring/Mirroring across chips
- Egress tagging/untagging selectable per port or by 802.1Q VLAN ID
- Port based VLANs supported in any combination across multiple chips
- Port States & BPDU handling for Spanning Tree
- 28 32-bit and 2 64-bit RMON Counters per port
- 88E6350R device Ports 5 and 6 support RGMII MAC Mode, RGMII PHY Mode, MII-MAC Mode (Forward), or MII-PHY Mode (Reverse—full-duplex) interface options
- 88E6350 device Ports 5 and 6 can support GMII PHY Mode, GMII MAC Mode (Port 6 only), MII-MAC Mode (Forward), MII-PHY Mode (Reverse—full-duplex), or RGMII MAC Mode, and RGMII PHY Mode interface options
- Integrated with five independent Auto-Crossover Gigabit Ethernet transceivers fully compliant with the applicable sections of IEEE802.3 and IEEE802.3u
- Flexible LED support for Link, Speed, Duplex Mode, Collision, and Tx/Rx Activities
- Supports a low-cost 25 MHz XTAL clock source
- Supports 4-Wire 93C56/93C66 or 2-Wire 24C01/24C02/24C04 EEPROMs
- Single chip integration of an 7 port GE QoS switch and memory in a 14 x 14 mm 128-pin TQFP (88E6350R) package, or a 20 x 20 mm 176-pin TQFP (88E6350 and 88E6351) package
- Low power dissipation P_{AVE} = 2.5W
- Available in Commercial grade temperature specification
- 88E6350R and 88E6351 available in Industrial grade temperature specification

Applications

- Gigabit AVB Ethernet broadband router with four 10/100/1000BASE-T LAN ports and one 10/100/1000 BASE-T WAN port
- 5 port Gigabit Ethernet AVB Switch
- Multi-dwelling unit interface gateway

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Figure 3: 88E6350R Device Pinout

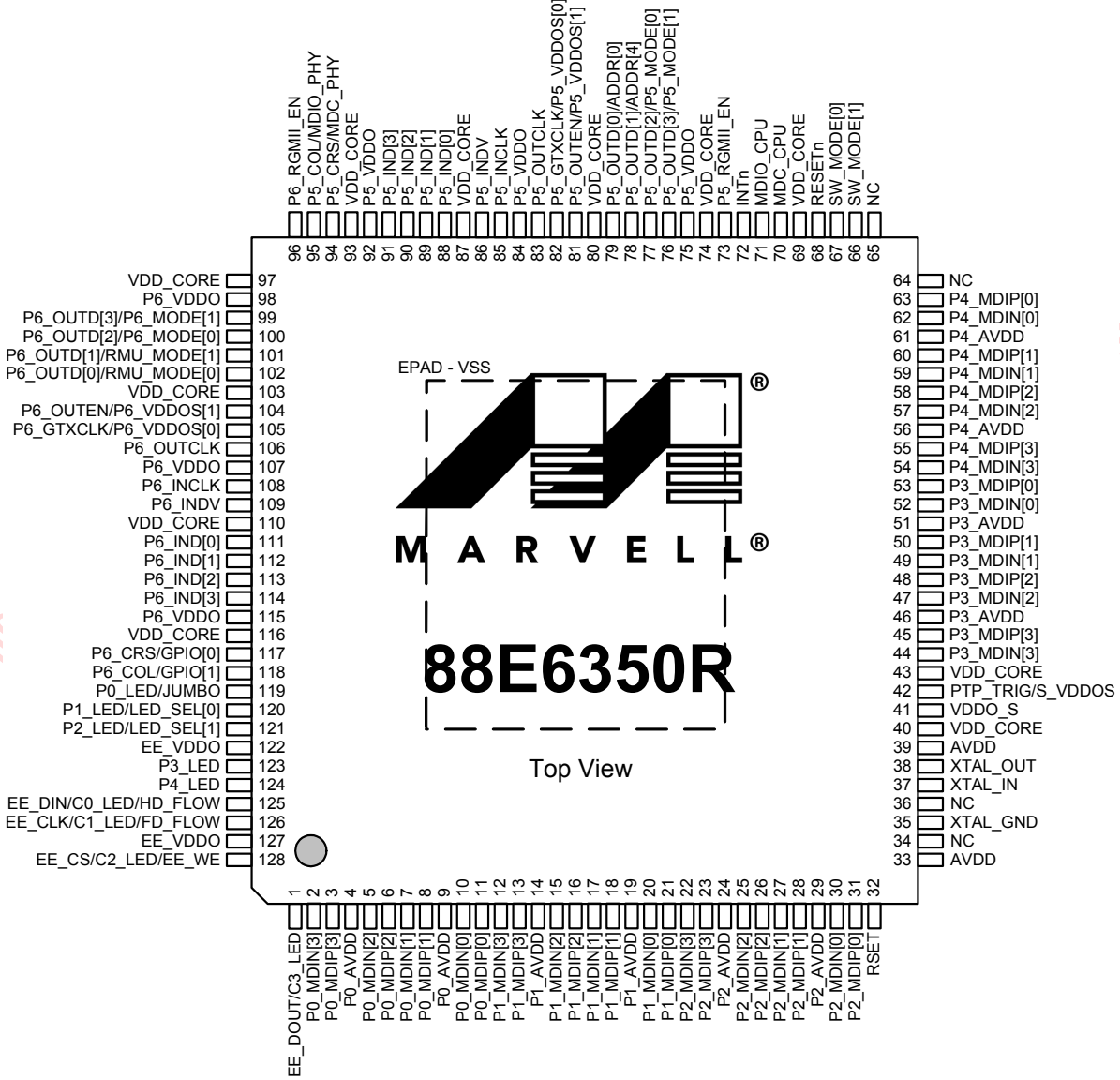


Figure 4: 88E6350 Device Pinout

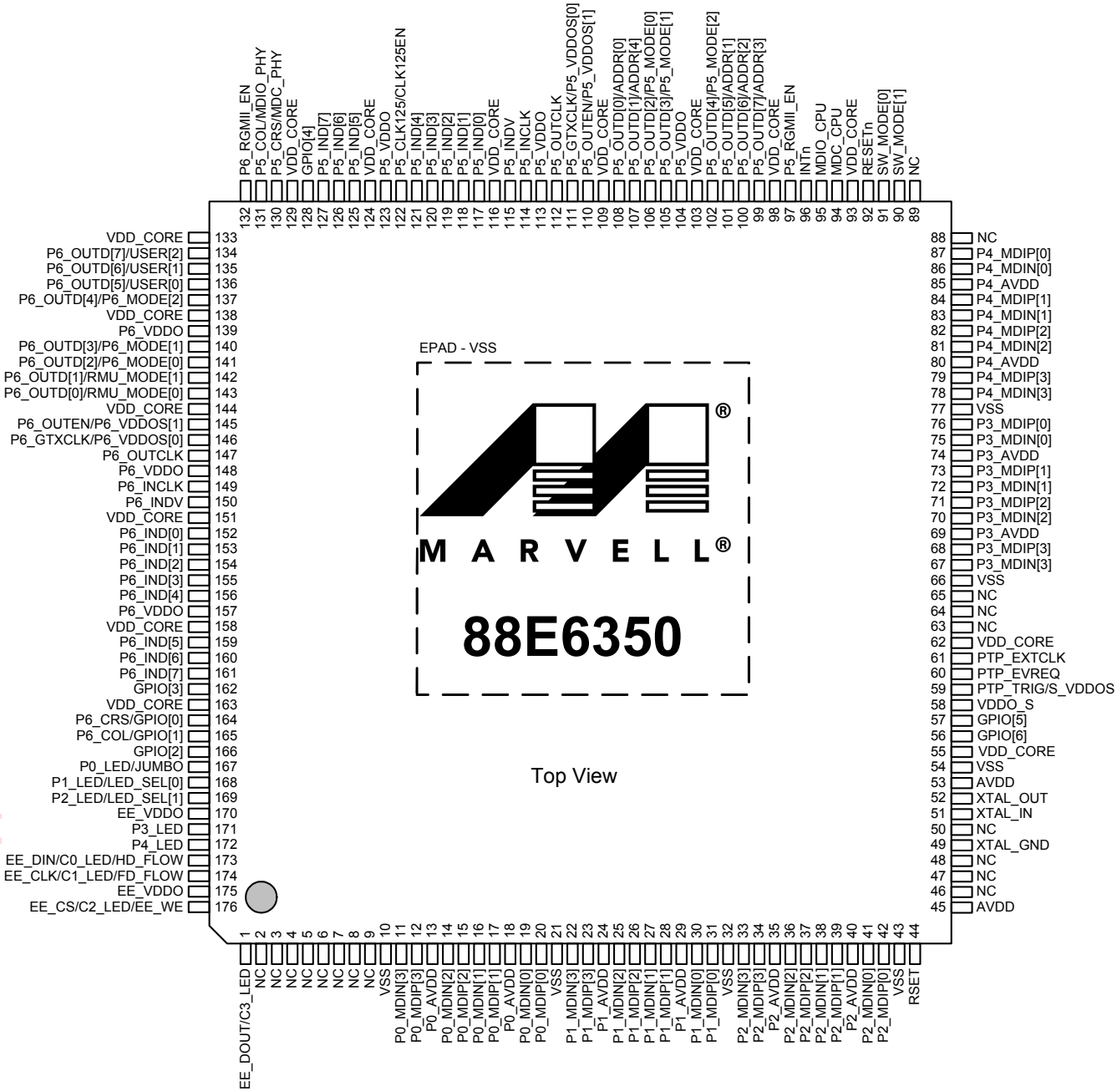
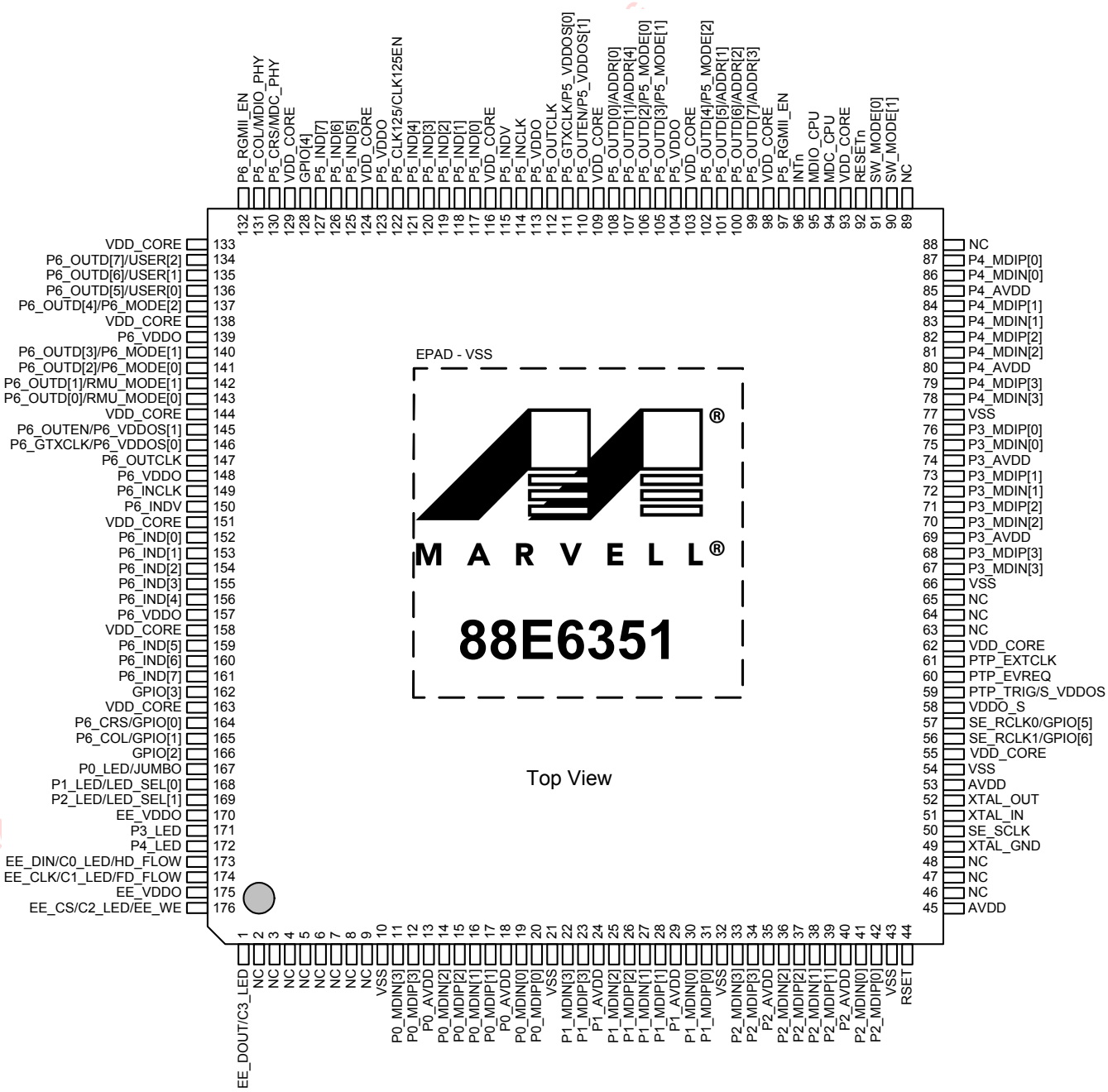


Figure 5: 88E6351 Device Pinout



1.1 Pin Description

Table 2: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability
Analog	Analog pin
H	Input with hysteresis

Note The MDI pins are internally terminated and do not need external termination resistors.

Table 3: Network 10/100/1000 PHY Interface (Ports 0 to 4)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
63 53 31 21 11 62 52 30 20 10	87 76 42 31 20 86 75 41 30 19	P4_MDIP[0] P3_MDIP[0] P2_MDIP[0] P1_MDIP[0] P0_MDIP[0] P4_MDIN[0] P3_MDIN[0] P2_MDIN[0] P1_MDIN[0] P0_MDIN[0]	I/O	Media Dependent Interface [0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] corresponds to BI_DA±. In MDIX configuration, MDIP/N[0] corresponds to BI_DB±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. **NOTE:** Unused MDI pins must be left floating.
60 50 28 18 8 59 49 27 17 7	84 73 39 28 17 83 72 38 27 16	P4_MDIP[1] P3_MDIP[1] P2_MDIP[1] P1_MDIP[1] P0_MDIP[1] P4_MDIN[1] P3_MDIN[1] P2_MDIN[1] P1_MDIN[1] P0_MDIN[1]	I/O	Media Dependent Interface [1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] corresponds to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. **NOTE:** Unused MDI pins must be left floating.
58 48 26 16 6 57 47 25 15 5	82 71 37 26 15 81 70 36 25 14	P4_MDIP[2] P3_MDIP[2] P2_MDIP[2] P1_MDIP[2] P0_MDIP[2] P4_MDIN[2] P3_MDIN[2] P2_MDIN[2] P1_MDIN[2] P0_MDIN[2]	I/O	Media Dependent Interface [2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] corresponds to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. **NOTE:** Unused MDI pins must be left floating.
55 45 23 13 3 54 44 22 12 2	79 68 34 23 12 78 67 33 22 11	P4_MDIP[3] P3_MDIP[3] P2_MDIP[3] P1_MDIP[3] P0_MDIP[3] P4_MDIN[3] P3_MDIN[3] P2_MDIN[3] P1_MDIN[3] P0_MDIN[3]	I/O	Media Dependent Interface [3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] corresponds to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. **NOTE:** Unused MDI pins must be left floating.

Table 4: Port Status LEDs (Ports 0 to 4)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
124 123 121 120 119	172 171 169 168 167	P4_LED P3_LED P2_LED /LED_SEL[1] P1_LED /LED_SEL[0] P0_LED /JUMBO	Typically O, PU	Parallel multiplexed LED outputs – one for each PHY port. These active low LED pins directly drive the port's LEDs supporting a range from 1 to 4 LEDs per PHY. The cathode of each LED is connected to these pins through a series current limiting resistor. The anode of each LED connects to one of the Cx_LED pins below. The LEDs can be configured to display many options as shown in Section 2.3. The LEDs are turned on whenever RESETn is low (as long as SW_MODE[1:0] is not CPU Attached/Disabled mode) so their functionality can be visually verified during PCB manufacturing testing. P[4:0]_LED are multifunction pins which are used to configure the device after a hardware reset. After reset is asserted, the Px_LED pins become inputs and the configuration information below is latched 1 ms after the rising edge of RESETn as follows: P[2:1]_LED: LED_SEL[1:0] 00 = Link/Activity with Speed by Blink Rate 01 = Link/Activity with Speed by 3 Colors 10 = Separate Link/Activity by Speed 11 = Link/Activity with Separate Speed **NOTE:** See Section 2.3.1 for a complete description of each of these LED Selections P0_LED: JUMBO 0 = 1522 Byte maximum frame size enabled on all ports 1 = 10K Byte Jumbo maximum frame size enabled on all ports **NOTE:** This configuration sets an initial value for each port's JumboMode register (Port offset 0x08). An EEPROM or CPU can override the above setting on a port by port basis. P[4:0]_LED are internally pulled high via a resistor so the pins can be left floating when unused. Use a 4.7 kohm resistor to VSS for a configuration low.

Table 4: Port Status LEDs (Ports 0 to 4) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
1	1	EE_DOUT /EE_IO /C3_LED	I/O, PU	Serial EEPROM data out from a 4-wire EEPROM device or Serial EEPROM data I/O to/from a 2-wire EEPROM device and Column 3 for the LEDs. EE_DOUT is serial EEPROM data referenced to EE_CLK used to receive (and send if 2-wire EEPROM) the EEPROM (address[1]/) data (to/) from the external serial EEPROM (if present). 2-wire EEPROMs require that this pin is connected to EE_VDDO with a 4.7 kohm pull-up resistor on the net. EE_DOUT is a multi-function pin which is also used to connect to the anode of LED column 3 for each port, if used (see P[4:0]_LED above). EE_DOUT is internally pulled high via a resistor so the pin can be left floating when unused.
128	176	EE_CS /C2_LED /EE_WE	Typically Output, PD	Serial EEPROM chip select and Column 2 for the LEDs. EE_CS is the 4-wire serial EEPROM chip select referenced to EE_CLK. It is used to enable the external 4-wire serial EEPROM (if present), and to delineate each data transfer. This pin is not used for 2-wire serial EEPROMs. EE_CS is a multi-function pin which is also used to connect to the anode of LED column 2 for each port, if used (see P[4:0]_LED above). It is also used to configure the device after a hardware reset. After reset is asserted, EE_CS becomes an input and the configuration information below is latched 1 ms after the rising edge of RESETn as follows: 0 = EEPROM is write protected 1 = EEPROM can be written to (see Section 10 in the 88E6350R/88E6350 Datasheet, Part 2 of 3: Switch Core) EE_CS is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to EE_VDDO for a configuration high.

Table 4: Port Status LEDs (Ports 0 to 4) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
126	174	EE_CLK /C1_LED /FD_FLOW	Typically Output, PD	Serial EEPROM clock and Column 1 for the LEDs. EE_CLK is the serial EEPROM clock reference output by the devices. It is used to shift the external serial EEPROM (if installed) to the next data bit so the default values of the internal registers can be overridden. EE_CLK is a multi-function pin which is also used to connect to the anode of LED column 1 for each port, if used (see P[4:0]_LED above). It is also used to configure the device after a hardware reset. After reset is asserted, EE_CLK becomes an input and the configuration information below is latched 1 ms after the rising edge of RESETn as follows: 0 = Disable full-duplex flow control on all full-duplex ports 1 = Enable advertisement of full-duplex flow control on all PHYs Full-duplex flow control requires support from the end station. It is supported on any full-duplex port that has Auto-Negotiation enabled, advertises that it supports Pause (i.e., FD_FLOW = 0x1 at reset), and sees that the end station also supports Pause (from data returned during Auto-Negotiation). EE_CLK is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to EE_VDDO for a configuration high.
125	173	EE_DIN /C0_LED /HD_FLOW	Typically Output, PD	Serial EEPROM data into the 4-wire EEPROM devices and Column 0 for the LEDs. EE_DIN is serial EEPROM data referenced to EE_CLK used to transmit the EEPROM command and address to the external 4-wire serial EEPROM (if present). This pin is not used for 2-wire serial EEPROMs. EE_DIN is a multi-function pin which is also used to connect to the anode of LED column 0 for each port, if used (see P[4:0]_LED above). It is also used to configure the device after a hardware reset. After reset is asserted, EE_DIN becomes an input and the configuration information below is latched 1 ms after the rising edge of RESETn as follows: 0 = Disable flow control on all half-duplex ports 1 = Enable “forced collision” flow control on all half-duplex port Half-duplex flow control is active on all half-duplex ports when enabled. EE_DIN is internally pulled low via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to EE_VDDO for a configuration high.

1. The address is sent out the EE_IO pin only for 2-wire EEPROMs.

Table 5: GMII/RGMII/MII Interface Enable (Port 5)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
73	97	P5_RGMII_EN	I, PU	Port 5's GMII/RGMII/MII interface enable (generically referred to as RGMII5). **NOTE:** Port 5 of the 88E6350R device does not support the GMII interface option. Setting this pin high will enable the output drivers on the RGMII5 interface pins, brings link up on Port 5 when P5_MODE pins are set to either 000, 001, 010 or 011 and enables the interface to transmit and receive data if the port's PortState bits allow it. **NOTE:** The 88E6350R device does not support P5_MODE of 000 (GMII). When this pin is low, RGMII5's output pins will be disabled (i.e., they are tri-stated). P5_RGMII_EN acts as Link status and is reflected in the registers (Port, Offset 0x0). P5_RGMII_EN is internally pulled high so the pin can be left floating to enable Port 5's interface.

Table 6: GMII/RGMII/MII Receive Interface (Port 5)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
85	114	P5_INCLK	I, PU	Input Clock. INCLK is a reference for INDV and IND. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending upon the speed of the port. In RGMII mode INCLK is used as RXC. INCLK is tri-stated during RESETn and it is internally pulled high so the pin can be left floating when unused.
-- -- -- -- 91 90 89 88	127 126 125 121 120 119 118 117	P5_IND[7] P5_IND[6] P5_IND[5] P5_IND[4] P5_IND[3] P5_IND[2] P5_IND[1] P5_IND[0]	I, PD	Input Data. IND[7:0] (or IND[3:0] where appropriate) receives the data octet or nibble to be sent into the switch. IND must be synchronous to INCLK. In 1000BASE GMII mode RXD[7:0] is used (not supported in the 88E6350R device). In 1000BASE RGMII, 200BASE, 100BASE and 10BASE modes RXD[3:0] is used and RXD[7:4] is ignored. In RGMII mode IND[3:0] are used as RXD[3:0]. The IND pins are internally pulled low via resistor so the pins can be left floating when unused.
86	115	P5_INDV	I, PD	Input Data Valid. Input Data Valid is used to indicate when IND[7:0] (or IND[3:0] where appropriate) contains frame information. INDV must be synchronous to INCLK. In RGMII mode INDV is used as RX_CTL. INDV is internally pulled low via resistor so the pin can be left floating when unused.
94	130	P5_CRS /MDC_PHY	I/O, PU	Carrier Sense or Management Data Clock, Master. Carrier sense is used to indicate that the carrier has been detected on the line. CRS is not synchronous to INCLK. CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is CRS when the port's MODE = 010, or 011. Management Data Clock, Master is the reference clock output for the serial management interface (SMI) that connects to an external SMI slave device, typically external PHYs. This pin is MDC_PHY when the port's MODE = 000, 001, 100, 101, 110 or 111. The Master SMI is used to access registers in any external SMI device (like a PHY) and it is controllable via switch registers. CRS is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the P5_MODE[2:0] pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P5_RGMII_EN.

Table 6: GMII/RGMII/MII Receive Interface (Port 5) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
95	131	P5_COL /MDIO_PHY	I/O, PU	Collision or Management Data I/O, Master. Collision is used to indicate both transmit and receive are occurring at the same time in half duplex mode. COL is not synchronous to INCLK. COL is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is COL when the port's MODE = 010 or 011. Management Data I/O, Master is used to transfer management data in and out of the device synchronously to MDC_PHY. This pin requires an external pull-up resistor in the range of 4.7K to 10K. This pin is MDIO_PHY when the port's MODE = 000, 001, 100, 101, 110 or 111. This device uses Device Addresses 0x05 to 0x06 to access the external PHYs for ports 5 to 6 respectively. The Master SMI is used to access registers in any external SMI device (like a PHY) and it is controllable via switch registers. COL is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the P5_MODE[2:0] pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P5_RGMII_EN.

Table 7: GMII/MII Transmit Interface (Port 5)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
82	111	P5_GTXCLK /P5_VDDOS[0]	Typically O, PU	Transmit Clock. GTXCLK is a reference for OUTEN and OUTD when the port is in GMII or RGMII mode. The speed of GTXCLK is 125 MHz and is normally only driven when the speed of the port is 1000 Mbps. GTXCLK can be configured to output a 50 MHz, 25 MHz or a 2.5 MHz clock so it can be used as a clock source for P5_INCLK and P5_OUTCLK when no other clock sources are available (see P5_MODE configuration in P5_OUTD's pins). In RGMII mode, GTXCLK is used as TXC. GTXCLK is tri-stated during RESETn and when RGMII_EN is low. It is internally pulled high so the pin can be left unconnected if not used. P5_GTXCLK is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: If P5_VDDOS[1], below on P5_OUTEN, is low at the rising edge of RESETn: 0 = The P5_VDDO pins are powered by 2.5 volts 1 = The P5_VDDO pins are powered by 3.3 volts If P5_VDDOS[1], below on P5_OUTEN, is high at the rising edge of RESETn: X = The P5_VDDO pins are powered by 1.8 volts See P5_VDDO for the list of pins that are powered by this rail. P5_GTXCLK is tri-stated during RESETn or when P5_RGMII_EN is low. GTXCLK is internally pulled high via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to VSS for a configuration low.

Table 7: GMII/MII Transmit Interface (Port 5) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
81	110	P5_OUTEN /P5_VDDOS[1]	Typically O, PD	Output Enable. Output enable is used to indicate when OUTD[7:0] (or OUTD[3:0] where appropriate) contains frame information. OUTEN is synchronous to GTXCLK in 1000BASE GMII and RGMII mode. It is synchronous to OUTCLK in 200BASE, 100BASE and 10BASE modes. In RGMII mode, OUTEN is used as TX_CTL. P5_OUTEN is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: 0 = The P5_VDDO pins are powered by 2.5 or 3.3 volts (P5_VDDOS[0], above on P5_GTXCLK, is used to select between 2.5 & 3.3 volts) 1 = The P5_VDDO pins are powered by 1.8 volts See P5_VDDO for the list of pins that are powered by this rail. P5_OUTEN is tri-stated during RESETn or when P5_RGMII_EN is low. OUTEN is internally pulled low via resistor so the pin can be left floating when unused. Use a 4.7K ohm resistor to VDDO for a configuration high.
83	112	P5_OUTCLK	I, PU	Output Clock. OUTCLK is an input clock reference for OUTEN and OUTD[3:0] when the port is in MII mode. The speed of OUTCLK is 50 MHz, 25 MHz or 2.5 MHz depending the speed of the port. OUTCLK is internally pulled high via resistor so the pin can be left floating when unused.

Table 7: GMII/MII Transmit Interface (Port 5) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
--	99	P5_OUTD[7] /ADDR[3]	Typically O, PD	Output Data. OUTD[7:0] (or OUTD[3:0] where appropriate) outputs the data octet or nibble to be transmitted from the switch. OUTD is synchronous to GTXCLK in 1000BASE GMII or RGMII mode. In 200BASE, 100BASE, and 10BASE modes, OUTD[3:0] is synchronous to OUTCLK and OUTD[7:4] is ignored. In RGMII mode, OUTD[3:0] are used as TXD[3:0]. P5_OUTD are multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn as follows: OUTD[4:2] = P5_MODE[2:0] (MODE[2] in 176 LQFP only) OUTD[1], [7:5], [0] = ADDR[4:0] (ADDR[3:1] in 176 LQFP only) P5_MODE[2:0] sets Port 5's Mode of operation as follows: 000 = GMII with P5_GTXCLK = 125 MHz[1] (1000BASE) 001 = RGMII with P5_GTXCLK = 125 MHz[2] (1000BASE) 010 = MII with P5_GTXCLK = 25 or 50 MHz[3] (100 or 200BASE) 011 = MII with P5_GTXCLK = 2.5 MHz (10BASE) 100 = Port 5 disabled (with its pins tri-stated[4]) 101 = Port 5 disabled (with its pins tri-stated[4]) 110 = Port 5 disabled (with its pins tri-stated[4]) 111 = Port 5 disabled (with its pins tri-stated[4]) ADDR[4:0] sets the device's SMI address. If ADDR[4:0] are all 0's the device is configured in single device addressing mode. **NOTE:** ADDR[3:1] are always zero in the 128 TQFP package. P5_OUTD pins are tri-stated during RESETn or when P5_RGMII_EN is low. OUTD pins are internally pulled low via resistor so the pins can be left floating when unused. Use a 4.7K ohm resistor to P5_VDDO for a configuration high.
--	100	P5_OUTD[6] /ADDR[2]		
--	101	P5_OUTD[5] /ADDR[1]		
--	102	P5_OUTD[4] /P5_MODE[2]		
76	105	P5_OUTD[3] /P5_MODE[1]		
77	106	P5_OUTD[2] /P5_MODE[0]		
78	107	P5_OUTD[1] /ADDR[4]		
79	108	P5_OUTD[0] /ADDR[0]		

1. The GMII mode on this port cannot be used to connect to an external GMII triple speed PHY They are intended to be connected to a full duplex gigabit device like a CPU port. P5_CRS and P5_COL are not tri-stated in this mode.
2. The RGMII mode on this port can be used to connect to a external RGMII triple speed PHY as long as the PHY's SMI address is set to 0x05 and the PHY's MDC & MDIO lines are connected to P5_CRS & P5_COL respectively.
3. In this mode P5_GTX_CLK comes up running at 25 MHz. It can be changed to 50 MHz for 200BASE mode speed by writing to a register (200BASE in Port offset 0x00 bit 6.
4. P5_CRS and P5_COL are not tri-stated in these modes.

Table 8: GMII/RGMII/MII Interface Enable (Port 6)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
96	132	P6_RGMII_EN	I, PU	Port 6's GMII/RGMII/MII interface enable (generically referred to as RGMII6). **NOTE:** Port 6 of the 88E6350R device does not support the GMII interface option. Setting this pin high will enable the output drivers on the RGMII6 interface pins, bring link up on Port 6 when P6_MODE pins are set to either 000, 001, 010 or 011, and enable the interface to transmit and receive data if the port's PortState bits allow it. **NOTE:** The 88E6350R device does not support P6_MODE of 000 (GMII) When this pin is low, RGMII6's output pins will be disabled (i.e., they are tri-stated). P6_RGMII_EN acts as Link status and is reflected in the registers (Port, Offset 0x0). P6_RGMII_EN is internally pulled high so the pin can be left floating to enable Port 6's interface.

Table 9: GMII/RGMII/MII Receive Interface (Port 6)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
108	149	P6_INCLK	I, PU	Input Clock. INCLK is a reference for INDV and IND. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz or 2.5 MHz depending upon the speed of the port. In RGMII mode, INCLK is used as RXC. INCLK is tri-stated during RESETn and it is internally pulled high so the pin can be left floating when unused.
-- -- -- -- 114 113 112 111	161 160 159 156 155 154 153 152	P6_IND[7] P6_IND[6] P6_IND[5] P6_IND[4] P6_IND[3] P6_IND[2] P6_IND[1] P6_IND[0]	I, PD	Input Data. IND[7:0] (or IND[3:0] where appropriate) receives the data octet or nibble to be sent into the switch. IND must be synchronous to INCLK. In 1000BASE GMII mode, RXD[7:0] is used (not supported in the 88E6350R device). In 1000 BASE RGMII, 200BASE, 100BASE and 10BASE modes RXD[3:0] is used and RXD[7:4] is ignored. In RGMII mode, IND[3:0] are used as RXD[3:0]. The IND pins are internally pulled low via resistor so the pins can be left floating when unused.
109	150	P6_INDV	I, PD	Input Data Valid. Input Data Valid is used to indicate when IND[7:0] (or IND[3:0] where appropriate) contains frame information. INDV must be synchronous to INCLK. In RGMII mode INDV is used as RX_CTL. INDV is internally pulled low via resistor so the pin can be left floating when unused.
117	164	P6_CRS /GPIO[0]	I, PU	Carrier Sense or General Purpose Input Output. Carrier sense is used to indicate carrier has been detected on the line. CRS is not synchronous to INCLK. CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is CRS when the port's MODE = 000, 010 or 011. GPIO[0] is a general purpose input/output pin whose direction and data is controllable via switch registers. This pin is GPIO[0] when the port's MODE = 001, 100, 101, 110 or 111. CRS is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the P6_MODE[2:0] pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P6_RGMII_EN.

Table 9: GMII/RGMII/MII Receive Interface (Port 6) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
118	165	P6_COL /GPIO[1]	I/O, PU	Collision or General Purpose Input Output. Collision is used to indicate both transmit and receive are occurring at the same time in half duplex mode. COL is not synchronous to INCLK. COL is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin is COL when the port's MODE = 000, 010 or 011. GPIO[1] is a general purpose input/output pin whose direction and data is controllable via switch registers. This pin is GPIO[1] when the port's MODE = 001, 100, 101, 110 or 111. COL is internally pulled high via resistor so the pin can be left floating when unused. The function of this pin is determined by the value of the P6_MODE[2:0] pins at the rising edge of RESETn (during RESETn this pin is an input). This pin is not tri-stated by P6_RGMII_EN.

Table 10: GMII/RGMII/MII Transmit Interface (Port 6)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
105	146	P6_GTXCLK /P6_VDDOS[0]	Typically O, PU	Transmit Clock. GTXCLK is a reference for OUTEN and OUTD when the port is in GMII or RGMII mode. The speed of GTXCLK is 125 MHz and is normally only driven when the speed of the port is 1000 Mbps. GTXCLK can be configured to output a 50 MHz, 25 MHz or a 2.5 MHz clock so it can be used as a clock source for P6_INCLK and P6_OUTCLK when no other clock sources are available (see P6_MODE configuration in P6_OUTD's pins). In RGMII mode, GTXCLK is used as TXC. GTXCLK is tri-stated during RESETn and when RGMII_EN is low. It is internally pulled high so the pin can be left unconnected if not used. P6_GTXCLK is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: If P6_VDDOS[1], below on P6_OUTEN, is low at the rising edge of RESETn: 0 = The P6_VDDO pins are powered by 2.5 volts 1 = The P6_VDDO pins are powered by 3.3 volts If P6_VDDOS[1], below on P6_OUTEN, is high at the rising edge of RESETn: X = The P6_VDDO pins are powered by 1.8 volts See P6_VDDO for the list of pins that are powered by this rail. P6_GTXCLK is tri-stated during RESETn or when P6_RGMII_EN is low. GTXCLK is internally pulled high via a resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to VSS for a configuration low.

Table 10: GMII/RGMII/MII Transmit Interface (Port 6) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
104	145	P6_OUTEN/ P6_VDDOS[1]	Typically O, PD	Output Enable. Output enable is used to indicate when OUTD[7:0] (or OUTD[3:0] where appropriate) contains frame information. OUTEN is synchronous to GTXCLK in 1000BASE GMII and RGMII mode. It is synchronous to OUTCLK in 200BASE, 100BASE, and 10BASE modes. In RGMII mode, OUTEN is used as TX_CTL. P6_OUTEN is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn: 0 = The P6_VDDO pins are powered by 2.5 or 3.3 volts (P6_VDDOS[0], above on P6_GTXCLK, is used to select between 2.5 & 3.3 volts) 1 = The P6_VDDO pins are powered by 1.8 volts See P6_VDDO for the list of pins that are powered by this rail. P6_OUTEN is tri-stated during RESETn or when P6_RGMII_EN is low. OUTEN is internally pulled low via resistor so the pin can be left floating when unused. Use a 4.7K ohm resistor to VDDO for a configuration high.
106	147	P6_OUTCLK	I, PU	Output Clock. OUTCLK is an input clock reference for OUTEN and OUTD[3:0] when the port is in MII mode. The speed of OUTCLK is 50 MHz, 25 MHz or 2.5 MHz depending the speed of the. OUTCLK is internally pulled high via resistor so the pin can be left floating when unused.

Table 10: GMII/RGMII/MII Transmit Interface (Port 6) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
--	134	P6_OUTD[7] /USER[2]	Typically O, PD	Output Data. OUTD[7:0] (or OUTD[3:0] where appropriate) outputs the data octet or nibble to be transmitted from the switch. OUTD is synchronous to GTXCLK in 1000BASE GMII or RGMII mode. In 200BASE, 100BASE and 10BASE modes OUTD[3:0] is synchronous to OUTCLK and OUTD[7:4] is ignored. In RGMII mode, OUTD[3:0] are used as TXD[3:0]. P6_OUTD are multi-function pins used to configure the device during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn as follows: OUTD[4:2] = P6_MODE[2:0] (MODE[2] in 176 LQFP only) OUTD[1:0] = RMU_MODE[1:0] OUTD[7:5] = USER[2:0] (USER[2:0] in 176 LQFP only) P6_MODE[2:0] sets Port 6's Mode of operation as follows: 000 = GMII with P6_GTXCLK = 125 MHz[1] (1000BASE) 001 = RGMII with P6_GTXCLK = 125 MHz[2] (1000BASE) 010 = MII with P6_GTXCLK = 25 or 50 MHz[3] (100 or 200BASE) 011 = MII with P6_GTXCLK = 2.5 MHz (10BASE) 100 = Port 6 disabled (with its pins tri-stated[4]) 101 = Port 6 disabled (with its pins tri-stated[4]) 110 = Port 6 disabled (with its pins tri-stated[4]) 111 = Port 6 disabled (with its pins tri-stated[4]) RMU_MODE[1:0] configures the Remote Management Unit (RMU) as follows: 000 = RMU disabled. 001 = RMU is enabled on Port 4 010 = RMU is enabled on Port 5 011 = Reserved for future use USER[2:0] are user definable configuration pins. The value on these pins is latched on the rising edge of RESETn and the latched values are accessible via switch registers. P6_OUTD pins are tri-stated during RESETn or when P6_RGMII_EN is low. OUTD pins are internally pulled low via resistor so the pins can be left floating when unused. Use a 4.7K ohm resistor to P6_VDDO for a configuration high.
--	135	P6_OUTD[6] /USER[1]		
--	136	P6_OUTD[5] /USER[0]		
--	137	P6_OUTD[4] /P6_MODE[2]		
99	140	P6_OUTD[3] /P6_MODE[1]		
100	141	P6_OUTD[2] /P6_MODE[0]		
101	142	P6_OUTD[1] /RMU_MODE[1]		
102	143	P6_OUTD[0] /RMU_MODE[0]		

1. The GMII mode on this port can be used to connect to an external GMII triple speed PHY as long as the PHY's SMI address is set to 0x06 and the PHY's MDC & MDIO lines are connected to P6_CRS & P6_COL respectively and Port 6 is configured in a mode such that its CRS/COL pins are the MDC_PHY/MDIO_PHY lines.
2. The RGMII mode on this port can be used to connect to a external RGMII triple speed PHY as long as the PHY's SMI address is set to 0x06 and the PHY's MDC & MDIO lines are connected to P6_CRS & P6_COL respectively and Port 6 is configured in a mode such that its CRS/COL pins are the MDC_PHY/MDIO_PHY lines.
3. In this mode P6_GTX_CLK comes up running at 25 MHz. It can be changed to 50 MHz for 200BASE mode speed by writing to a register (200BASE in Port offset 0x00 bit 6.
4. P6_CRS and P6_COL are not tri-stated in these modes.

Table 11: System and Register Access Interface

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
70	94	MDC_CPU	I	Management Data Clock, Slave. MDC_CPU is the reference clock input for the serial management interface (SMI) that connects to an external SMI master, typically a CPU. A continuous clock stream is not expected. The maximum frequency supported is 20.0 MHz. The CPU's SMI interface is used to access the device's registers but it cannot be used until the device's INTn pin becomes active low (indicating the Register Loader is done processing the EEPROM or that no EEPROM was present). MDC_CPU is internally pulled high via a resistor so it can be left floating when unused.
71	95	MDIO_CPU	I/O	Management Data I/O, Slave. MDIO_CPU is used to transfer management data in and out of the device synchronously to MDC_CPU. This pin requires an external pull-up resistor in the range of 4.7K to 10K. The device uses one or all of the 32 possible SMI port addresses (two modes are supported). The address(es) that are used are selectable using the P5_OUTD/ADDR configuration pins. MDIO_CPU is internally pulled high via a resistor so it can be left floating when unused.
72	96	INTn	D	INTn is an active low, open drain pin that is asserted to indicate an unmasked interrupt event occurred. A single external pull-up resistor is required somewhere on this interrupt net for it to go high when it is inactive. The INTn pin will go active low which indicates the MDC_CPU/MDIO_CPU interface is available for use. The CPU SMI interface cannot be used while the Register Loader is processing an EEPROM, if one is present.
68	92	RESETn	I	Hardware reset. Active low. The device is configured during reset. When RESETn is low some configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or some time after. Other configuration pins are active during RESETn low and become inputs after RESETn rises. These pins latch their configuration data sometime after RESETn rises and then these pins become their defined function. Refer to Section 3.6.1, Receiver AC Characteristics, on page 79 for Reset and Configuration Timing details.

Table 12: Switch Configuration Interface

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
66 67	90 91	SW_MODE[1] SW_MODE[0]	I, PU I, PD	Switch Mode. These pins are used to configure the device after reset. Switch Mode pins work as follows: 00 = Test mode 01 = Reserved 10 = Unmanaged/Forwarding mode (default) 11 = CPU Attached/Disabled mode The Test mode should not be used as it is meant for chip testing only. Unmanaged/Forwarding mode does the following: • Turns on all the LEDs during RESETn low • Sets all switch port's PortStates to Forwarding • Sets all the PHYs in the Powered Up state CPU Attached/Disabled mode does the following: • Prevents the LEDs from turning on during RESETn low • Sets all switch port's PortState to Disabled • Sets all the PHYs in the Powered Down state All modes, except the Test mode, will look for and read any EEPROM that may be present. If no EEPROM is present or when the end of the EEPROM data is reached (by an EEPROM Halt op code) the device's INTn pin will go active low. This indicates the Register Loader is done accessing the registers and that the CPU SMI register interface is now available for use (see MDC_CPU & MDIO_CPU). The CPU Attached mode is required for managed switches and routers. This mode allows the CPU to boot and properly configure the switch before allowing packets to flow. This is critical for routers as WAN packets must not flow directly to the LAN ports, and vice versa (which they would in the Unmanaged mode until the CPU booted and changed the switch's configuration). The PHYs are powered down so they will not link until the CPU is ready to communicate with its link partners. The LEDs do not turn on so they can be used by software. The Unmanaged mode is required when no CPU is available to manage or bring up the switch. This mode gets the switch ready without the need of an EEPROM, although an EEPROM can also be used. In this mode the LEDs are turned on so they can be inspected easily during manufacturing testing. SW_MODE[1:0] are not latched on the rising edge of RESETn and they must remain static for proper device operation. They are internally set to 10 so the pins can be left unconnected to enable the Unmanaged/Forwarding mode.

Table 13: GPIO

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
-- -- --	166 162 128	GPIO[2] GPIO[3] GPIO[4]	I/O, PU	General Purpose Input/Output. At RESETn, these pins become General Purpose Input Output (GPIO[2], GPIO[3], and GPIO[4]) whose direction is set as an input. As a GPIO, these pin's direction and data is controllable via switch registers. GPIO[2], GPIO[3], and GPIO[4] are internally pulled high via resistor so the pins can be left floating when unused.
--	57	GPIO[5] (SE_RCLK0/GPIO[5] for the 88E6351 device only)	I/O, PD	General Purpose Input/Output. At RESETn, this pin becomes a General Purpose Input Output (GPIO[5]) whose direction is set as an input. As a GPIO this pin's direction and data is controllable via switch registers. GPIO[5] is internally pulled low via resistor so the pin can be left floating when unused. For the 88E6351 device, SE_RCLK0/GPIO[5] is a multifunction pin that is also used to determine the Power on reset value for the SE_RCLK0 pin. See Table 15 for SE_RCLK0 details.
--	56	GPIO[6] (SE_RCLK1/GPIO[6] for the 88E6351 device only)	I/O, PD	General Purpose Input/Output. At RESETn, this pin becomes a General Purpose Input Output (GPIO[6]) whose direction is set as an input. As a GPIO this pin's direction and data is controllable via switch registers. GPIO[6] is internally pulled low via resistor so the pin can be left floating when unused. For the 88E6351 device, SE_RCLK1/GPIO[6] is a multifunction pin that is also used to determine the Power on reset value for the SE_RCLK1 pin. See Table 15 for SE_RCLK1 details.

Table 14: Precise Timing Protocol (PTP) Timing Application Interface (TAI)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
--	61	PTP_EXTCLK	I, PU	Precise Timing Protocol External Clock input. The precise time core inside the device needs a time stamping clock (typically 125 MHz) to time stamp the PTP event messages. For high accuracy applications the time stamping clock which is syntonized (frequency locked) with respect to the PTP Grand Master clock can be supplied into the device via this pin. The device does not assume anything about the method and apparatus used for syntonizing the clocks. At RESETn the PTP time stamping clock runs off of the internal 125 MHz free running clock. Use PTP Ext Clk Sel register (AVB Policy Global offset 0x0B) to select this pin as the PTP time stamping clock. PTP_EXTCLK is internally pulled high via resistor so the pin can be left floating when unused.
--	60	PTP_EVREQ	I, PD	Precise Timing Protocol Event Request. This pin acts as a Precise Timing Protocol engine Event request input. The device assists in keeping track of external events on a given system by observing a low to high transition on this pin and capturing the 32-bit PTP Global Time Register into the Event Capture Register (TAI Global Status register, Offset 0x0A & 0x0B) on that rising edge. Please refer to section xxx for further detailed options on the Event Capture interface support. PTP_EVREQ is internally pulled low via resistor so the pin can be left floating when unused.

Table 14: Precise Timing Protocol (PTP) Timing Application Interface (TAI) (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
42	59	PTP_TRIG/ S_VDDOS	I/O, PU	Precise Timing Protocol Trigger Generate. This pin acts as a Precise Timing Protocol engine Trigger generate output. The device assists in keeping external devices on the system to be PTP synchronized by generating timing based pulse(s) on this pin. The output can be configured both in pulse and/or clock mode. The timing of the output is controlled by a 32-bit PTP TriggerGenAmt (TAI Global Control, Offset 0x2 & 0x3), an enable bit TrigGenReq (TAI Global Config, Offset 0x0) and a mode bit TrigMode (TAI Global Config, Offset 0x1). PTP_TRIG/S_VDDOS is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin becomes an input, and the configuration information below is latched at the rising edge of RESETn: 0 = The VDDO_S pins are powered by 2.5 volts 1 = The VDDO_S pins are powered by 3.3 volts See VDDO_S in Table 17 for the list of pins that are powered by this rail. Please refer to section xxx for further detailed options on the Trigger Generate interface support. PTP_TRIG/S_VDDOS is internally pulled high via resistor so the pin can be left floating when unused. Use a 4.7 kohm resistor to VSS for a configuration low.

Table 15: Synchronous Ethernet Interface (88E6351 Device only)

88E6351 Pin #	Pin Name	Pin Type	Description
57	SE_RCLK0 /GPIO[5]	O, PD	Synchronous Ethernet Primary recovered clock output. This pin can output a 25 MHz clock that is frequency matched to any one of the physical PHYs receiver blocks inside the device. In this mode this pin is always 25 MHz regardless of the PHY's link speed.Both the primary and the secondary recovered clock outputs can be configured to output the same frequency clock output (i.e., they are both connected to the same PHY). The Power on reset output value for this pin is GPIO[5]. See Table 13 for GPIO[5] details. See section??? on how to configure this pin as a recovered clock. At RESETn, this pin becomes a General Purpose Input Output (GPIO[5]) whose direction is set as an input. As a GPIO this pin's direction and data is controllable via switch registers. SE_RCLK0/GPIO[5] is internally pulled low via resistor so the pin can be left floating when unused.
56	SE_RCLK1 /GPIO[6]	O, PD	Synchronous Ethernet Secondary recovered clock output. This pin can output a 25 MHz clock that is frequency matched to any one of the physical PHYs receiver blocks inside the device. In this mode this pin is always 25 MHz regardless of the PHY's link speed. Both the primary and the secondary recovered clock outputs can be configured to output the same frequency clock output (i.e., they are both connected to the same PHY). The Power on reset output value for this pin is GPIO[6]. See Table 13 for GPIO[6] details. See section??? on how to configure this pin as a recovered clock. At RESETn, this pin becomes a General Purpose Input Output (GPIO[6]) whose direction is set as an input. As a GPIO this pin's direction and data is controllable via switch registers. SE_RCLK1/GPIO[6] is internally pulled low via resistor so the pin can be left floating when unused.

Table 16: Reference and Clock

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
32	44	RSET	Analog	Resistor Current reference. A 4.99 kohm 1% resistor is placed between the RSET and VSS. This resistor is used to set an internal bias reference current.
37	51	XTAL_IN	I	25 MHz system reference clock input provided from the board. The clock source can come from an external crystal or an external oscillator. This is the only clock required. Refer to Section 3.6.2, Clock Timing, on page 80 for timing requirements. The XTAL_IN pin requires a 1.8V input.
38	52	XTAL_OUT	O	System reference clock output provided to the board. This output can only be used to drive an external crystal. It cannot be used to drive external logic. If an external oscillator is used this pin should be left unconnected.
35	49	XTAL_GND	I	Analog Ground for the XTAL. The external crystal circuit requires capacitors to be connected to the XTAL_IN and XTAL_OUT pins. The other side of these capacitors must be connected to this pin instead of being directly connected to the ground plane. Use as short of a trace as possible.
--	50 (88E6351 Device only)	SE_SCLK	I	Synchronous Ethernet Source Clock. This is a 25 MHz reference clock which can be used as a synchronous clock input from the board or system. Each PHY, via a PHY register, can select this clock input as its reference clock input instead of using the default XTAL_IN input. SE_CLK is internally pulled low via a resistor so the pin can be left floating when unused.
--	122	CLK125 /CLK125EN	O, PD	125 MHz Clock. When enabled, CLK125 is a free running 125 MHz clock that is asynchronous to all other clocks. CLK125 will always be 125 MHz unless its disabled, then its tri-stated. CLK125 is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin become an input and the configuration information below is latched at the rising edge of RESETn as follows: 0 = CLK125 is disabled (tri-stated) 1 = CLK125 is enabled CLK125 is tri-stated during RESETn. CLK125 is internally pulled low via resistor so the pin can be left floating when unused. Use a 4.7K ohm resistor to P5_VDDO for a configuration high. **NOTE:** CLK125 is powered by the P5_VDDO power rail.

Table 17: Power and Ground

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
75 84 92	104 113 123	P5_VDDO	Power	Power to pin numbers 88 to 131 in the 176-pin TQFP, pin numbers 64 to 95 in the 128-pin TQFP. P5_VDDO must be connected to 3.3V for 3.3V I/O, 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and P5_VDDOS[1:0] must be configured accordingly – see P5_OUTEN & P5_GTXCLK).
98 107 115	139 148 157	P6_VDDO	Power	Power to pin numbers 132 to 165 in the 176-pin TQFP, pin numbers 96 to 118 in the 128-pin TQFP. P6_VDDO must be connected to 3.3V for 3.3V I/O, 2.5V for 2.5V I/O or 1.8V for 1.8V I/O (and P6_VDDOS[1:0] must be configured accordingly – see P6_OUTEN & P6_GTXCLK).
122 127	170 175	EE_VDDO	Power	Power to pin numbers 166 to 176 and pin 1 in the 176-pin TQFP, pin numbers 119 to 128 and pin 1 in the 128-pin TQFP. EE_VDDO must be connected to 3.3V for 3.3V I/O or 2.5V for 2.5V I/O.
61 56 51 46 29 24 19 14 9 4	85 80 74 69 40 35 29 24 18 13	P4_AVDD P4_AVDD P3_AVDD P3_AVDD P2_AVDD P2_AVDD P1_AVDD P1_AVDD P0_AVDD P0_AVDD	Power	1.8V Power to analog core used to power each Gig PHY interface.
33 39	45 53	AVDD	Power	Gigabit PHY 1.8V power to analog core used to power the on-chip PLL.
41	58	VDDO_S	Power	2.5V or 3.3V power for I/O pins. For the 88E6350R device (128-pin TQFP package): For 2.5V operation, this pin must be connected to 2.5V and pin 42 must be pulled low with 4.7 kohm resistor. For 3.3V operation, this pin must be connected to 3.3V and pin 42 must be pulled high with 4.7 kohm resistor. If pin 42 is not used, this pin must be connected to either 1.8V, 2.5V, or 3.3V. For the 88E6350 device and the 88E6351R device (176-pin TQFP package): This pin is 2.5V or 3.3V power for I/O pins 56 - 61. For 2.5V operation, this pin must be connected to 2.5V and pin 59 must pulled low with a 4.7 kohm resistor. For 3.3V operation, this pin must be connected to 3.3V and pin 59 must be pulled high with 4.7 kohm resistor. If pins 56 - 61 are not used, this pin must be connected to either 1.8V, 2.5V, or 3.3V.

Table 17: Power and Ground (Continued)

88E6350R Pin #	88E6350/ 88E6351 Pin #	Pin Name	Pin Type	Description
40 43 69 74 80 87 93 97 103 110 116	55 62 93 98 103 109 116 124 129 133 138 144 151 158 163	VDDO_CORE	Power	1.0V power to the digital core.
--	10 21 32 43 54 66 77	VSS	Ground	Ground to device. These ground pins are used to isolate the neighboring high speed interfaces from one another.
EPAD	EPAD	VSS	Ground	Ground to device. The 88E6350R device is packaged in a 128-pin TQFP package with an EPAD (exposed die pad) on the bottom of the package. The 88E6350/88E6351 devices are packaged in a 176-pin TQFP package with an EPAD (exposed die pad) on the bottom of the package. This EPAD must be soldered to VSS as it is the main VSS connection on the device. The location and dimensions of the EPAD can be found in Section 4, Package Mechanical Dimensions, on page 97. See the Marvell® EPAD Layout Guidelines Application Note for EPAD layout details.

Table 18: No Connect

88E6350R Pin #	88E6350/ Pin #	88E6351 Pin #	Pin Name	Pin Type	Description
34 36 64 65	2 3 4 5 6 7 8 9 46 47 48 50 63 64 65 88 89	2 3 4 5 6 7 8 9 46 47 48 63 64 65 88 89	NC	--	No Connect. Do not connect these pins to anything. These pins must be left unconnected.

1.2 88E6350R/88E6350/88E6351 Device Pin Assignment List

Table 19: 88E6350R Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
33	AVDD
39	AVDD
126	EE_CLK/C1_LED/FD_FLOW
128	EE_CS/C2_LED/EE_WE
125	EE_DIN/C0_LED/HD_FLOW
1	EE_DOUT/C3_LED
122	EE_VDDO
127	EE_VDDO
72	INTn
70	MDC_CPU
71	MDIO_CPU
34	NC
36	NC
64	NC
65	NC
4	P0_AVDD
9	P0_AVDD
119	P0_LED/JUMBO
10	P0_MDIN[0]
7	P0_MDIN[1]
5	P0_MDIN[2]
2	P0_MDIN[3]
11	P0_MDIP[0]
8	P0_MDIP[1]
6	P0_MDIP[2]
3	P0_MDIP[3]
14	P1_AVDD
19	P1_AVDD
120	P1_LED/LED_SEL[0]
20	P1_MDIN[0]
17	P1_MDIN[1]
15	P1_MDIN[2]
12	P1_MDIN[3]
21	P1_MDIP[0]
18	P1_MDIP[1]
16	P1_MDIP[2]
13	P1_MDIP[3]
24	P2_AVDD
29	P2_AVDD
121	P2_LED/LED_SEL[1]
30	P2_MDIN[0]
27	P2_MDIN[1]
25	P2_MDIN[2]
22	P2_MDIN[3]
31	P2_MDIP[0]
28	P2_MDIP[1]
26	P2_MDIP[2]
23	P2_MDIP[3]
46	P3_AVDD
51	P3_AVDD
123	P3_LED

Pin Number	Pin Name
52	P3_MDIN[0]
49	P3_MDIN[1]
47	P3_MDIN[2]
44	P3_MDIN[3]
53	P3_MDIP[0]
50	P3_MDIP[1]
48	P3_MDIP[2]
45	P3_MDIP[3]
56	P4_AVDD
61	P4_AVDD
124	P4_LED
62	P4_MDIN[0]
59	P4_MDIN[1]
57	P4_MDIN[2]
54	P4_MDIN[3]
63	P4_MDIP[0]
60	P4_MDIP[1]
58	P4_MDIP[2]
55	P4_MDIP[3]
95	P5_COL/MDIO_PHY
94	P5_CRS/MDC_PHY
82	P5_GTXCLK/P5_VDDOS[0]
85	P5_INCLK
88	P5_IND[0]
89	P5_IND[1]
90	P5_IND[2]
91	P5_IND[3]
86	P5_INDV

Pin Number	Pin Name
83	P5_OUTCLK
79	P5_OUTD[0]/ADDR[0]
78	P5_OUTD[1]/ADDR[4]
77	P5_OUTD[2]/P5_MODE[0]
76	P5_OUTD[3]/P5_MODE[1]
81	P5_OUTEN/P5_VDDOS[1]
73	P5_RGMII_EN
75	P5_VDDO
84	P5_VDDO
92	P5_VDDO
118	P6_COL/GPIO[1]
117	P6_CRS/GPIO[0]
105	P6_GTXCLK/P6_VDDOS[0]
108	P6_INCLK
111	P6_IND[0]
112	P6_IND[1]
113	P6_IND[2]
114	P6_IND[3]
109	P6_INDV
106	P6_OUTCLK
102	P6_OUTD[0]/RMU_MODE[0]
101	P6_OUTD[1]/RMU_MODE[1]
100	P6_OUTD[2]/P6_MODE[0]
99	P6_OUTD[3]/P6_MODE[1]
104	P6_OUTEN/P6_VDDOS[1]
96	P6_RGMII_EN
98	P6_VDDO
107	P6_VDDO

Pin Number	Pin Name
115	P6_VDDO
42	PTP_TRIG/S_VDDOS
68	RESETn
32	RSET
67	SW_MODE[0]
66	SW_MODE[1]
40	VDD_CORE
43	VDD_CORE
69	VDD_CORE
74	VDD_CORE
80	VDD_CORE
87	VDD_CORE
93	VDD_CORE
97	VDD_CORE
103	VDD_CORE
110	VDD_CORE
116	VDD_CORE
41	VDDO_S
EPAD	VSS
35	XTAL_GND
37	XTAL_IN
38	XTAL_OUT

Table 20: 88E6350 Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
45	AVDD
53	AVDD
174	EE_CLK/C1_LED/FD_FLOW
176	EE_CS/C2_LED/EE_WE
173	EE_DIN/C0_LED/HD_FLOW
1	EE_DOUT/C3_LED
170	EE_VDDO
175	EE_VDDO
166	GPIO[2]
128	GPIO[4]
162	GPIO[3]
57	GPIO[5]
56	GPIO[6]
96	INTn
94	MDC_CPU
95	MDIO_CPU
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
46	NC
47	NC
48	NC
50	NC
63	NC
64	NC
65	NC
88	NC
89	NC
13	P0_AVDD
18	P0_AVDD
167	P0_LED/JUMBO
19	P0_MDIN[0]
16	P0_MDIN[1]
14	P0_MDIN[2]
11	P0_MDIN[3]
20	P0_MDIP[0]
17	P0_MDIP[1]
15	P0_MDIP[2]
12	P0_MDIP[3]
24	P1_AVDD
29	P1_AVDD
168	P1_LED/LED_SEL[0]
30	P1_MDIN[0]
27	P1_MDIN[1]
25	P1_MDIN[2]
22	P1_MDIN[3]
31	P1_MDIP[0]
28	P1_MDIP[1]
26	P1_MDIP[2]
23	P1_MDIP[3]
35	P2_AVDD
40	P2_AVDD
169	P2_LED/LED_SEL[1]
41	P2_MDIN[0]
38	P2_MDIN[1]

Pin Number	Pin Name
36	P2_MDIN[2]
33	P2_MDIN[3]
42	P2_MDIP[0]
39	P2_MDIP[1]
37	P2_MDIP[2]
34	P2_MDIP[3]
69	P3_AVDD
74	P3_AVDD
171	P3_LED
75	P3_MDIN[0]
72	P3_MDIN[1]
70	P3_MDIN[2]
67	P3_MDIN[3]
76	P3_MDIP[0]
73	P3_MDIP[1]
71	P3_MDIP[2]
68	P3_MDIP[3]
80	P4_AVDD
85	P4_AVDD
172	P4_LED
86	P4_MDIN[0]
83	P4_MDIN[1]
81	P4_MDIN[2]
78	P4_MDIN[3]
87	P4_MDIP[0]
84	P4_MDIP[1]
82	P4_MDIP[2]
79	P4_MDIP[3]
122	P5_CLK125/CLK125EN
131	P5_COL/MDIO_PHY
130	P5_CRS/MDC_PHY

Pin Number	Pin Name
111	P5_GTXCLK/P5_VDDOS[0]
114	P5_INCLK
117	P5_IND[0]
118	P5_IND[1]
119	P5_IND[2]
120	P5_IND[3]
121	P5_IND[4]
125	P5_IND[5]
126	P5_IND[6]
127	P5_IND[7]
115	P5_INDV
112	P5_OUTCLK
108	P5_OUTD[0]/ADDR[0]
107	P5_OUTD[1]/ADDR[4]
106	P5_OUTD[2]/P5_MODE[0]
105	P5_OUTD[3]/P5_MODE[1]
102	P5_OUTD[4]/P5_MODE[2]
101	P5_OUTD[5]/ADDR[1]
100	P5_OUTD[6]/ADDR[2]
99	P5_OUTD[7]/ADDR[3]
110	P5_OUTEN/P5_VDDOS[1]
97	P5_RGMII_EN
104	P5_VDDO
113	P5_VDDO
123	P5_VDDO
165	P6_COL/GPIO[1]
164	P6_CRS/GPIO[0]
146	P6_GTXCLK/P6_VDDOS[0]
149	P6_INCLK
152	P6_IND[0]
153	P6_IND[1]

Pin Number	Pin Name
154	P6_IND[2]
155	P6_IND[3]
156	P6_IND[4]
159	P6_IND[5]
160	P6_IND[6]
161	P6_IND[7]
150	P6_INDV
147	P6_OUTCLK
143	P6_OUTD[0]/RMU_MODE[0]
142	P6_OUTD[1]/RMU_MODE[1]
141	P6_OUTD[2]/P6_MODE[0]
140	P6_OUTD[3]/P6_MODE[1]
137	P6_OUTD[4]/P6_MODE[2]
136	P6_OUTD[5]/USER[0]
135	P6_OUTD[6]/USER[1]
134	P6_OUTD[7]/USER[2]
145	P6_OUTEN/P6_VDDOS[1]
132	P6_RGMII_EN
139	P6_VDDO
148	P6_VDDO
157	P6_VDDO
60	PTP_EVREQ
61	PTP_EXTCLK
59	PTP_TRIG/S_VDDOS
92	RESETn
44	RSET
91	SW_MODE[0]
90	SW_MODE[1]
55	VDD_CORE
62	VDD_CORE
93	VDD_CORE

Pin Number	Pin Name
98	VDD_CORE
103	VDD_CORE
109	VDD_CORE
116	VDD_CORE
124	VDD_CORE
129	VDD_CORE
133	VDD_CORE
138	VDD_CORE
144	VDD_CORE
151	VDD_CORE
158	VDD_CORE
163	VDD_CORE
58	VDDO_S
10	VSS
21	VSS
32	VSS
43	VSS
54	VSS
66	VSS
77	VSS
EPAD	VSS
49	XTAL_GND
51	XTAL_IN
52	XTAL_OUT

Table 21: 88E6351 Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
45	AVDD
53	AVDD
174	EE_CLK/C1_LED/FD_FLOW
176	EE_CS/C2_LED/EE_WE
173	EE_DIN/C0_LED/HD_FLOW
1	EE_DOUT/C3_LED
170	EE_VDDO
175	EE_VDDO
166	GPIO[2]
128	GPIO[4]
162	GPIO[3]
96	INTn
94	MDC_CPU
95	MDIO_CPU
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
46	NC
47	NC
48	NC
63	NC
64	NC
65	NC
88	NC
89	NC

Pin Number	Pin Name
13	P0_AVDD
18	P0_AVDD
167	P0_LED/JUMBO
19	P0_MDIN[0]
16	P0_MDIN[1]
14	P0_MDIN[2]
11	P0_MDIN[3]
20	P0_MDIP[0]
17	P0_MDIP[1]
15	P0_MDIP[2]
12	P0_MDIP[3]
24	P1_AVDD
29	P1_AVDD
168	P1_LED/LED_SEL[0]
30	P1_MDIN[0]
27	P1_MDIN[1]
25	P1_MDIN[2]
22	P1_MDIN[3]
31	P1_MDIP[0]
28	P1_MDIP[1]
26	P1_MDIP[2]
23	P1_MDIP[3]
35	P2_AVDD
40	P2_AVDD
169	P2_LED/LED_SEL[1]
41	P2_MDIN[0]
38	P2_MDIN[1]
36	P2_MDIN[2]
33	P2_MDIN[3]
42	P2_MDIP[0]
39	P2_MDIP[1]

Pin Number	Pin Name
37	P2_MDIP[2]
34	P2_MDIP[3]
69	P3_AVDD
74	P3_AVDD
171	P3_LED
75	P3_MDIN[0]
72	P3_MDIN[1]
70	P3_MDIN[2]
67	P3_MDIN[3]
76	P3_MDIP[0]
73	P3_MDIP[1]
71	P3_MDIP[2]
68	P3_MDIP[3]
80	P4_AVDD
85	P4_AVDD
172	P4_LED
86	P4_MDIN[0]
83	P4_MDIN[1]
81	P4_MDIN[2]
78	P4_MDIN[3]
87	P4_MDIP[0]
84	P4_MDIP[1]
82	P4_MDIP[2]
79	P4_MDIP[3]
122	P5_CLK125/CLK125EN
131	P5_COL/MDIO_PHY
130	P5_CRS/MDC_PHY
111	P5_GTXCLK/P5_VDDOS[0]
114	P5_INCLK
117	P5_IND[0]
118	P5_IND[1]

Pin Number	Pin Name
119	P5_IND[2]
120	P5_IND[3]
121	P5_IND[4]
125	P5_IND[5]
126	P5_IND[6]
127	P5_IND[7]
115	P5_INDV
112	P5_OUTCLK
108	P5_OUTD[0]/ADDR[0]
107	P5_OUTD[1]/ADDR[4]
106	P5_OUTD[2]/P5_MODE[0]
105	P5_OUTD[3]/P5_MODE[1]
102	P5_OUTD[4]/P5_MODE[2]
101	P5_OUTD[5]/ADDR[1]
100	P5_OUTD[6]/ADDR[2]
99	P5_OUTD[7]/ADDR[3]
110	P5_OUTEN/P5_VDDOS[1]
97	P5_RGMII_EN
104	P5_VDDO
113	P5_VDDO
123	P5_VDDO
165	P6_COL/GPIO[1]
164	P6_CRS/GPIO[0]
146	P6_GTXCLK/P6_VDDOS[0]
149	P6_INCLK
152	P6_IND[0]
153	P6_IND[1]
154	P6_IND[2]
155	P6_IND[3]
156	P6_IND[4]
159	P6_IND[5]

Pin Number	Pin Name
160	P6_IND[6]
161	P6_IND[7]
150	P6_INDV
147	P6_OUTCLK
143	P6_OUTD[0]/RMU_MODE[0]
142	P6_OUTD[1]/RMU_MODE[1]
141	P6_OUTD[2]/P6_MODE[0]
140	P6_OUTD[3]/P6_MODE[1]
137	P6_OUTD[4]/P6_MODE[2]
136	P6_OUTD[5]/USER[0]
135	P6_OUTD[6]/USER[1]
134	P6_OUTD[7]/USER[2]
145	P6_OUTEN/P6_VDDOS[1]
132	P6_RGMII_EN
139	P6_VDDO
148	P6_VDDO
157	P6_VDDO
60	PTP_EVREQ
61	PTP_EXTCLK
59	PTP_TRIG/S_VDDOS
92	RESETn
44	RSET
57	SE_RCLK0/GPIO[5]
56	SE_RCLK1/GPIO[6]
50	SE_SCLK
91	SW_MODE[0]
90	SW_MODE[1]
55	VDD_CORE

Pin Number	Pin Name
62	VDD_CORE
93	VDD_CORE
98	VDD_CORE
103	VDD_CORE
109	VDD_CORE
116	VDD_CORE
124	VDD_CORE
129	VDD_CORE
133	VDD_CORE
138	VDD_CORE
144	VDD_CORE
151	VDD_CORE
158	VDD_CORE
163	VDD_CORE
58	VDDO_S
10	VSS
21	VSS
32	VSS
43	VSS
54	VSS
66	VSS
77	VSS
EPAD	VSS
49	XTAL_GND
51	XTAL_IN
52	XTAL_OUT

2 Application Examples

2.1 Examples using the 88E6350R/88E6350/88E6351 Device

Figure 6: AVB Gigabit Firewall Router with four LAN Ports and one WAN Port using Two Ports for a CPU

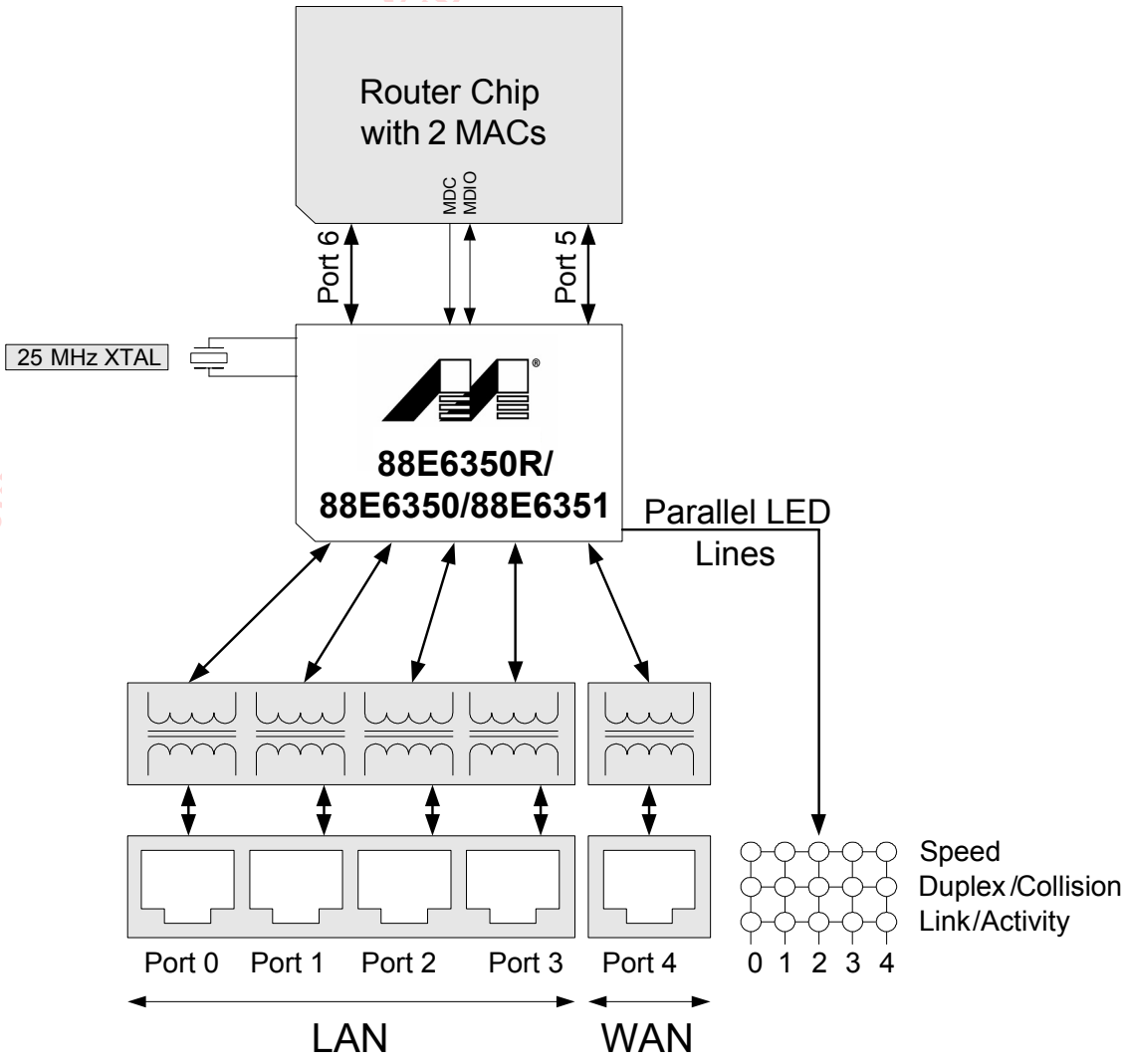
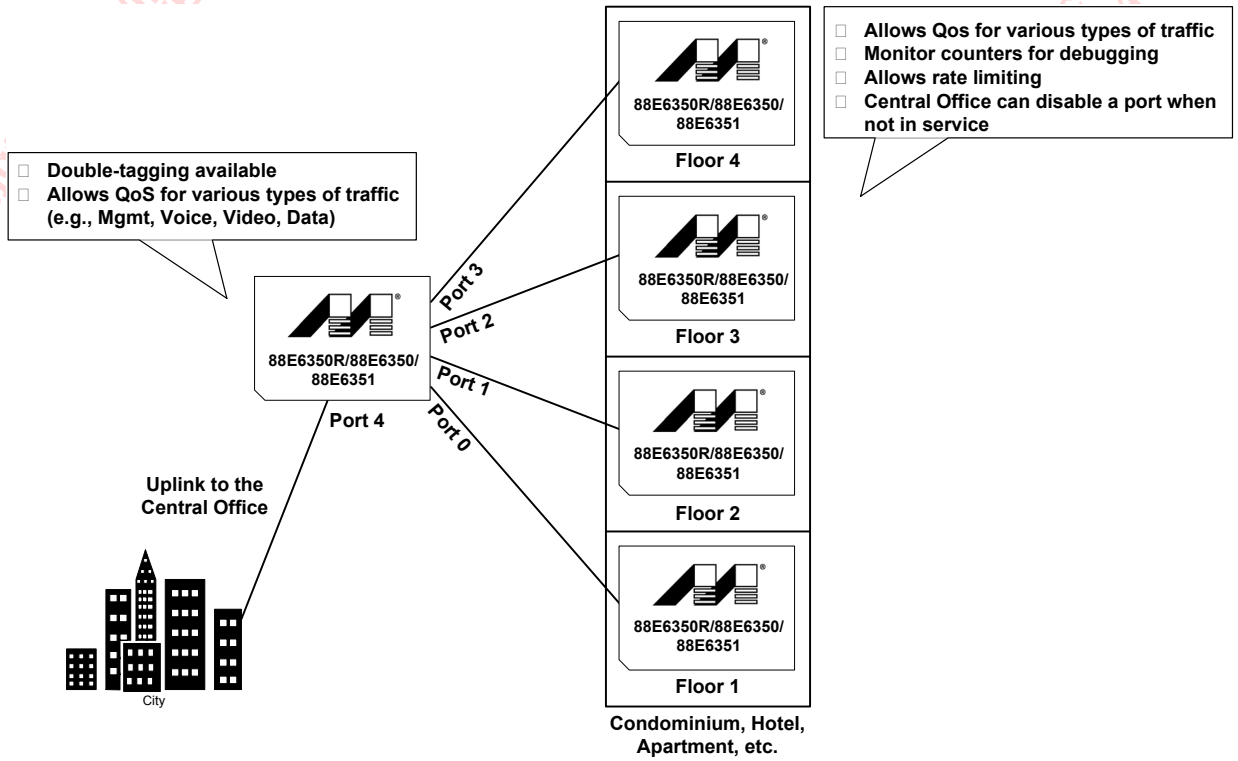


Figure 7: 5 Port AVB Gigabit Ethernet with TAI Interface

Figure 8: AVB Enabled Multi-dwelling Unit Interface Gateway



2.2 Device Physical Interfaces

The device contains a number of interfaces that support copper media. Table 22 lists the interfaces supported on each port of the 88E6350R/88E6350/88E6351 device. Refer to the diagrams further in this section for connection details.

Table 22: 88E6350R/88E6350/88E6351 Device Interfaces

Port	10BASE-T 100BASE-T	1000BASE-T	GMII	RGMII	MII/ 200 Mbps MII
0-4	x	x			
5-6 (88E6350R)				x	x
5-6 (88E6350)			x	x	x

2.2.1 10/100/1000 PHY Interface

Ports 0 to 4 on the device support a 10/100/1000 PHY interface. In the device, this interface supports 10BASE-T, 100BASE-TX, and 1000BASE-T copper IEEE standards. The MAC inside the switch works the same way regardless of the external interface being used. Each PHY's Link, Speed, Duplex and Flow Control information is directly communicated to the MAC it is attached to so the MAC tracks, or follows, the mode the PHY links up in. A detailed description of the PHY functional and register description is covered in "88E6350R/88E6350/88E6351 Datasheet Part 3 of 3: Gigabit PHYs".

2.2.2 MII 200 Mbps Mode

Port 5 and Port 6 of the device's GMII/MII interfaces can run at a data rate of 200 Mbps, full-duplex. Do not select this mode unless the MAC on the other end of the MII interface can also run at double speed rate. Both PHY (reverse MII) and MAC (forward MII) 200 Mbps modes are supported. When the 200 Mbps PHY mode is selected, the output MII clocks run at 50[1] MHz rate. These is no change in the format of the data, it just runs faster. When the 200 Mbps MAC mode is selected, an external 50 MHz ±50 ppm clock source must be supplied. Again, the format of the data is not changed.

2.2.3 Digital Interface Options

The (G)MII digital interface supports many different modes defined in the following sections. The mode to use is configured once at reset by external pull-up resistors connected to the P5_MODE[2:0] and P6_MODE[2:0] pins. See Table 7 and Table 10 for more information. If Port 5 or Port 6 is not connected to any device, the port should be disabled.

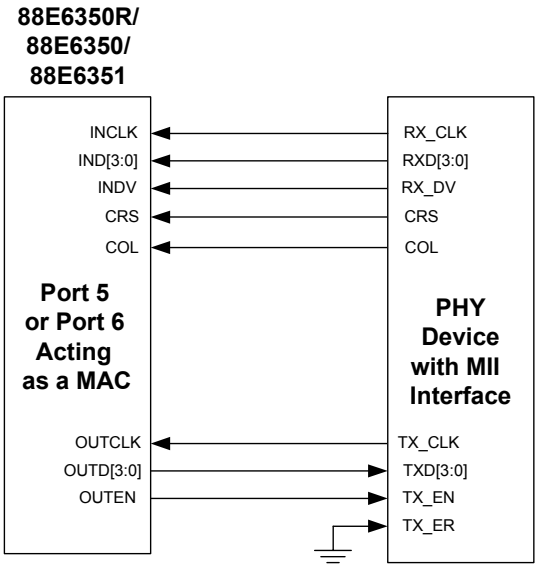
Note (G)MII PHY mode and (G)MII MAC mode are discussed in the following sections. Electrically, there is no difference since the GMII Interface uses source synchronous clocks. Each concept is discussed separately since the port supports being connected to an external PHY (GMII MAC mode - where the port looks like a MAC supporting 10/100/1000 Mbps) or to an external MAC (GMII PHY mode where the port looks like a PHY supporting 1000 Mbps only).

1. 50 MHz is enabled by writing to Port offset 0x00 bit 6.

2.2.3.1 MII MAC Mode

The MII MAC Mode, sometimes called 'Forward MII', configures Port 5 or Port 6's GMAC inside the devices to act as a MAC so it can be directly connected to an external MII-based PHY. In this mode, the devices receive the interface clocks (Px_OUTCLK and Px_INCLK) from the PHY and will work at any frequency from DC to 50 MHz. The two clocks can be asynchronous with each other. Both full- and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII MAC mode is compliant with IEEE 802.3 clause 22. (**Note:** The MII requires only four data bits in each direction so only the lower four data bits are used). P5_MODE or P6_MODE should be set correctly at reset (see Table 7 and Table 10) to select this configuration and the PHY's SMI address must be set to 0x05 for Port 5 or 0x06 for Port 6 for auto-negotiation to operate correctly.

Figure 9: MII MAC Interface Pins

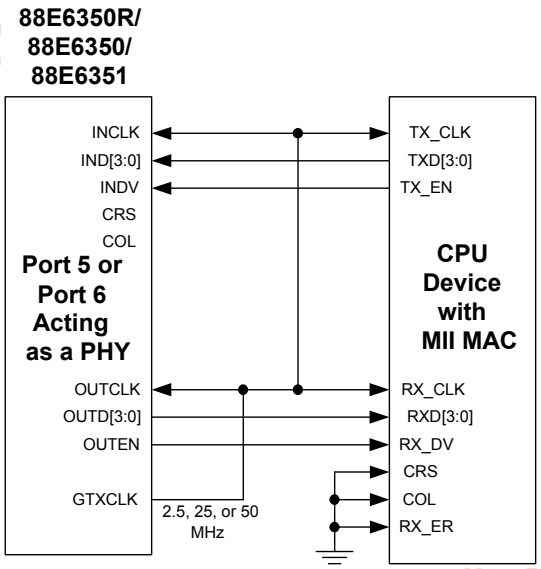


2.2.3.2 MII PHY Mode

The MII PHY Mode, sometimes called 'Reverse MII', configures Port 5 or Port 6's GMAC inside the device to act as a PHY so that it can be directly connected to an external MAC. In this mode, the devices drive the interface clocks (INCLK and OUTCLK for both MACs) from its GTXCLK pin so the appropriate GTXCLK frequency must be selected. GTX_CLK is used as a generic asynchronous clock source, but it is recommended that there are not more than four loads on GTX_CLK. For connection to more than four loads (that is, connection for use with Port 5), buffer Port 6's GTX_CLK, or use a generic oscillator. Only full-duplex modes are supported (since CRS and COL are not driven by the devices outputs) and must match the mode of the link partner's MAC.

The MII PHY mode is compliant with IEEE 802.3 clause 22 in full-duplex mode (**Note**: The MII requires only four data bits in each direction so only the lower four data bits on the devices are used). At reset, P5_MODE and P6_MODE should be set for the appropriate speed —see Table 7 and Table 10. In this mode, there is no external PHY for Port 5 or Port 6, and so Port 5 or Port 6 is skipped by the PPU. In Reverse MII mode, initially the link status is down requiring the system software to force the port's link up to enable the port.

Figure 10: MII PHY Interface Pins

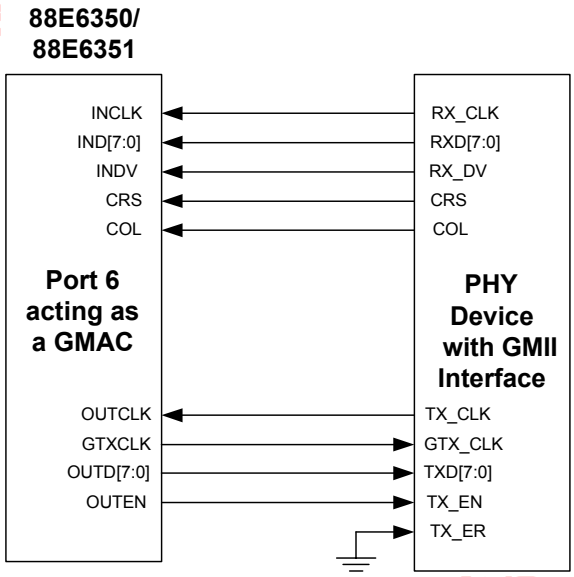


2.2.3.3 GMII MAC Mode

The GMII MAC Mode, sometimes called 'Forward GMII', configures Port 6's GMAC inside the device to act as a gigabit MAC (GMAC) so that it can be directly connected to an external GMII-based Gigabit PHY. In this mode, the devices receive the interface clocks (OUTCLK and INCLK) from the PHY but generate GTXCLK for the PHY. 10 Mbps, 100 Mbps or 1000 Mbps is supported in this configuration. Full- and half-duplex modes are supported at 10 Mbps or 100 Mbps. Full-duplex is supported at 1000 Mbps. The speed and mode in the external PHY's auto-negotiation must be restricted from advertising the 1000BASE, half-duplex case as the GMAC inside the devices do not support that mode. This is done automatically by the PHY Polling Unit (PPU) inside the devices. GMII MAC mode is compliant with IEEE 802.3 clause 28. P6_MODE should be set to GMII mode at reset (see Table 10) for this configuration and the PHY's SMI address must be set to 0x06 for Port 6 for auto-negotiation to operate correctly.

A triple speed interface is supported in GMII MAC mode (i.e., 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up, the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's settings. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The interface pins will track the speed that the MAC is set to.

Figure 11: GMII MAC Interface Pins

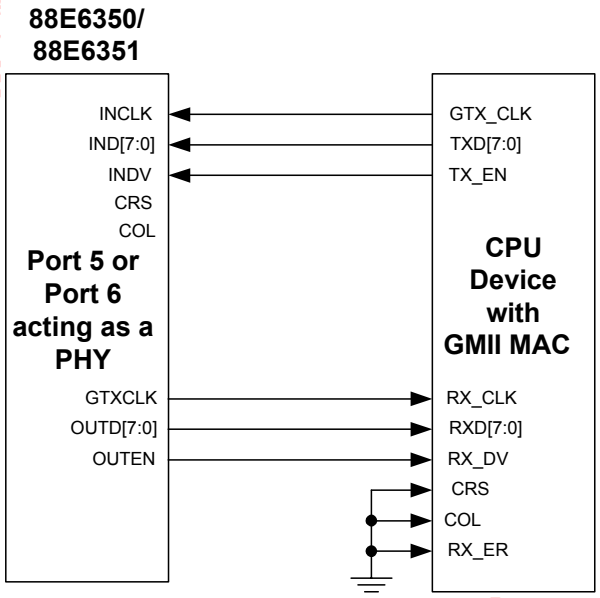


2.2.3.4 GMII PHY Mode

The GMII PHY Mode, sometimes called 'Reverse GMII', configures Port 5's or Port 6's GMAC inside the device to act as a gigabit PHY so that it can be directly connected to an external GMAC. In this mode, the devices drive the transmit interface clock (GTXCLK) and accept the receive interface clock (INCLK). Only gigabit full-duplex mode is supported and must match the mode of the link partner's GMAC. The GMII PHY mode is compliant with IEEE 802.3 clause 28 in gigabit full-duplex. P5_MODE and P6_MODE should be set to GMII mode at reset (see Table 7 and Table 10). In this mode, there is no external PHY for Port 5 or Port 6, so Port 5 or Port 6 are skipped by the PHY Polling Unit (PPU). Initially, the link status is configured down requiring the system software to force the port's link up to enable the port (in the PCS Control Register).

This configuration is identical to the GMII MAC Mode described above except that a CPU is connected instead of a PHY. The lack of an external PHY device restricts the interface to a gigabit speed only with the link initially being down. This allows the CPU time to initialize itself before it enables the switch port connected to it by forcing link up in the switch port's MAC (in the port's PCS Control Register - offset 0x01).

Figure 12: GMII PHY Interface Pins

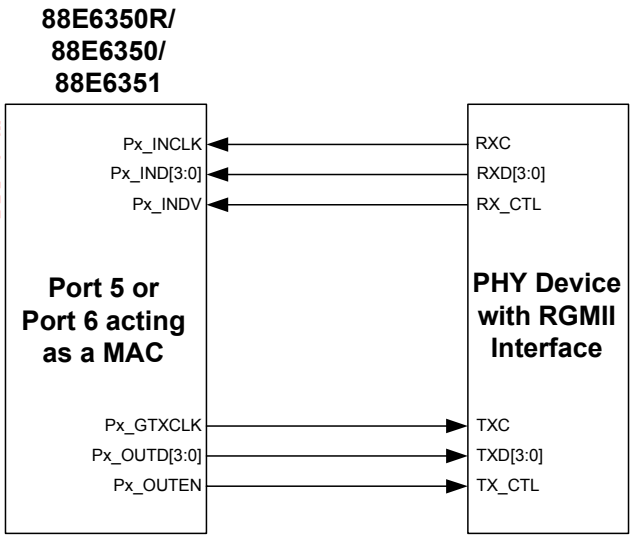


2.2.3.5 RGMII MAC Mode

The RGMII MAC Mode configures Port 5's or Port 6's GMAC to act as a Reduced Gigabit Media Independent Interface (RGMII) so that it can be directly connected to an external RGMII-based Gigabit PHY. When the RGMII mode is selected, transmit control (P5_OUTEN or P6_OUTEN) is presented on both clock edges of P5_GTXCLK or P6_GTXCLK. Receive control (P5_INDV or P6_INDV) is presented on both clock edges of P5_INCLK or P6_INCLK.

A triple speed interface is supported in RGMII MAC mode (i.e., 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up, the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's settings. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The interface pins will track the speed that the MAC is set to.

Figure 13: RGMII MAC Interface Pins

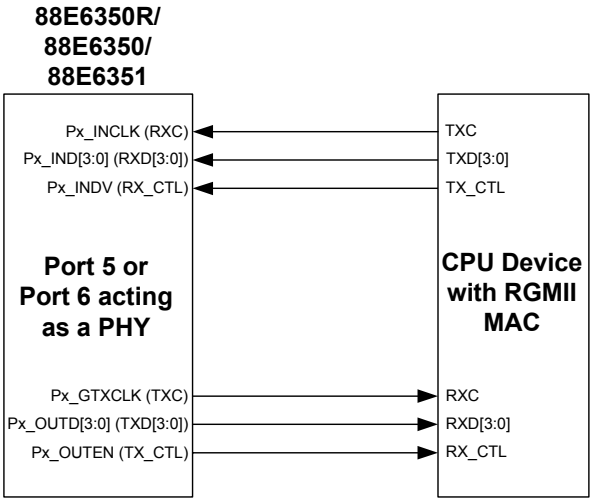


2.2.3.6 RGMII PHY Mode

The RGMII PHY Mode configures Port 5's or Port 6's GMAC to act as a Reduced Gigabit Media Independent Interface (RGMII) so that it can be directly connected to an external RGMII-based Gigabit MAC inside a CPU. When the RGMII mode is selected, transmit control (P5_OUTEN or P6_OUTEN) is presented on both clock edges of P5_GTXCLK or P6_GTXCLK. Receive control (P5_INDV or P6_INDV) is presented on both clock edges of P5_INCLK or P6_INCLK.

This configuration is identical to the GMII MAC Mode described above except that a CPU is connected instead of a PHY. The lack of an external PHY device restricts the interface to a gigabit speed only with the link initially being down. This allows the CPU time to initialize itself before it enables the switch port connected to it by forcing link up in the switch port's MAC (in the port's PCS Control register - offset 0x01)

Figure 14: RGMII PHY Interface Pins



2.2.4 PHY Polling Unit (PPU)

The devices contain a PHY Polling Unit (PPU) to transfer Link, Speed, Duplex and Pause information from an external PHY to its associated MAC (the internal PHYs use a direct approach such that this information is transferred even if the Port's PHYDetect bit is zero - Port offset 0x00). The PPU can perform this job only if the SMI address of the external PHY matches the physical port number it is connected to in the switch (i.e., the PHY connected to Port 4 uses SMI address 0x04, the PHY connected to Port 5 uses SMI address 0x05, etc.).

If the PPU is disabled on a port (i.e., the port's PHYDetect bit is zero), software must perform the job of setting the switch MAC's mode to the mode of the PHY (for the external PHYs) by forcing the MAC's link, speed, duplex and pause settings (in the port's PCS Control Register - offset 0x01) based upon what it sees in the PHY's registers. Link up must be the last mode register set and link down must be the first mode register cleared (i.e., the port's speed, duplex and pause modes must only be changed while the port's link is down).

Even though the PPU has full access to the external and internal PHY's registers, software can access all of the PHY registers at any time by using the SMI Command and Data registers (Global 2, offsets 0x18 and 0x19).

Note

On previous devices, the PPU could be disabled by a PPUEn bit (Global 1, offset 0x04) and the PPU's state could be read in the PPUState bits (Global 1, offset 0x00). These bits exist and function the same in this device, but they are documented differently or as Reserved bits as this is no longer the recommended way to access the PHY registers (use the SMI Command and Data registers instead - Global 2, offsets 0x18 and 0x19). The PPUEn and PPUState bits will physically be changed in future devices to match this documentation.

2.3 LED Interface

The 88E6350R/88E6350/88E6351 device uses a matrixed LED interface allowing each port to have up to four LEDs. Each port has a common signal (Px_LED) connected to the anode of its LEDs. The cathode of each LED is connected to a single column signal (Cx_LED).

The column signals (Cx_LED) are also shared with the EEPROM interface, and the architecture allows for the LEDs and EEPROM to operate at the same by time multiplexing the bus into 5 time cycles (C0_LED, C1_LED, C2_LED, C3_LED, and EEPROM). This prevents EEPROM access from interfering with LED operation and vice versa.

Although an EEPROM is not required for most applications, the 88E6350R/88E6350/88E6351 device supports either 2 or 4 wire EEPROMs. Figure 15 and Figure 16 illustrate typical LED connections with 2 or 4 wire EEPROM connections.

Figure 15: Four LEDs plus a 4 wire EEPROM

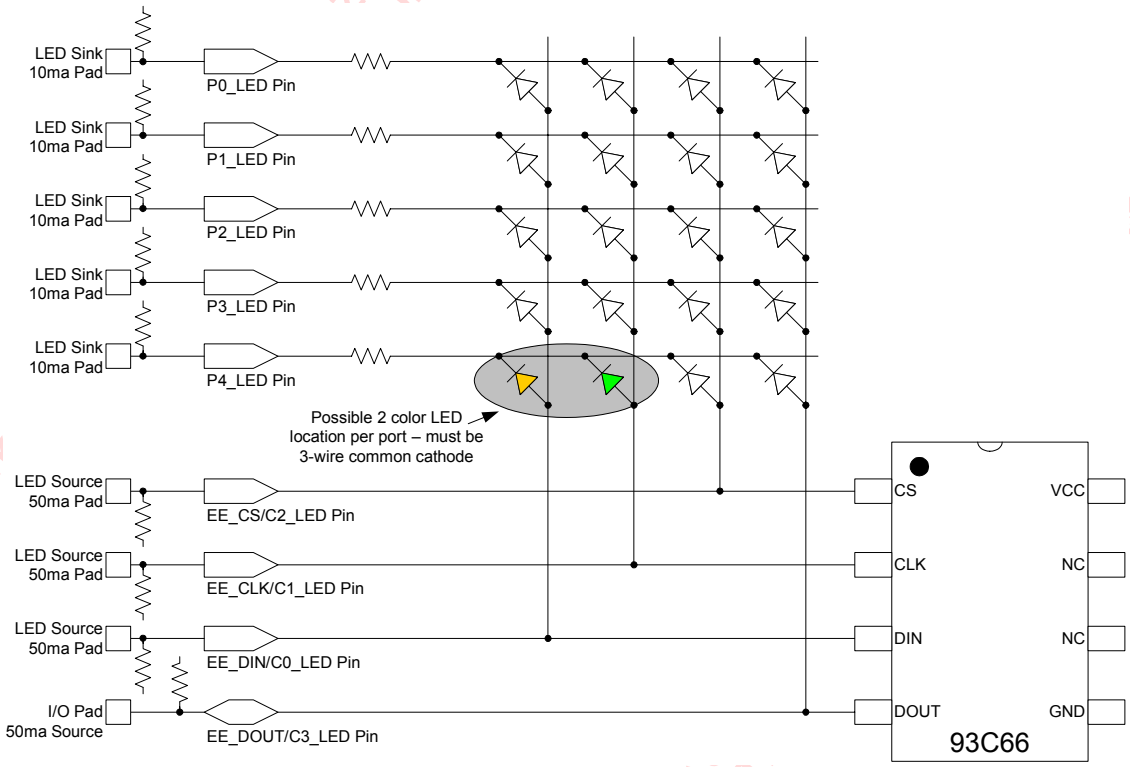
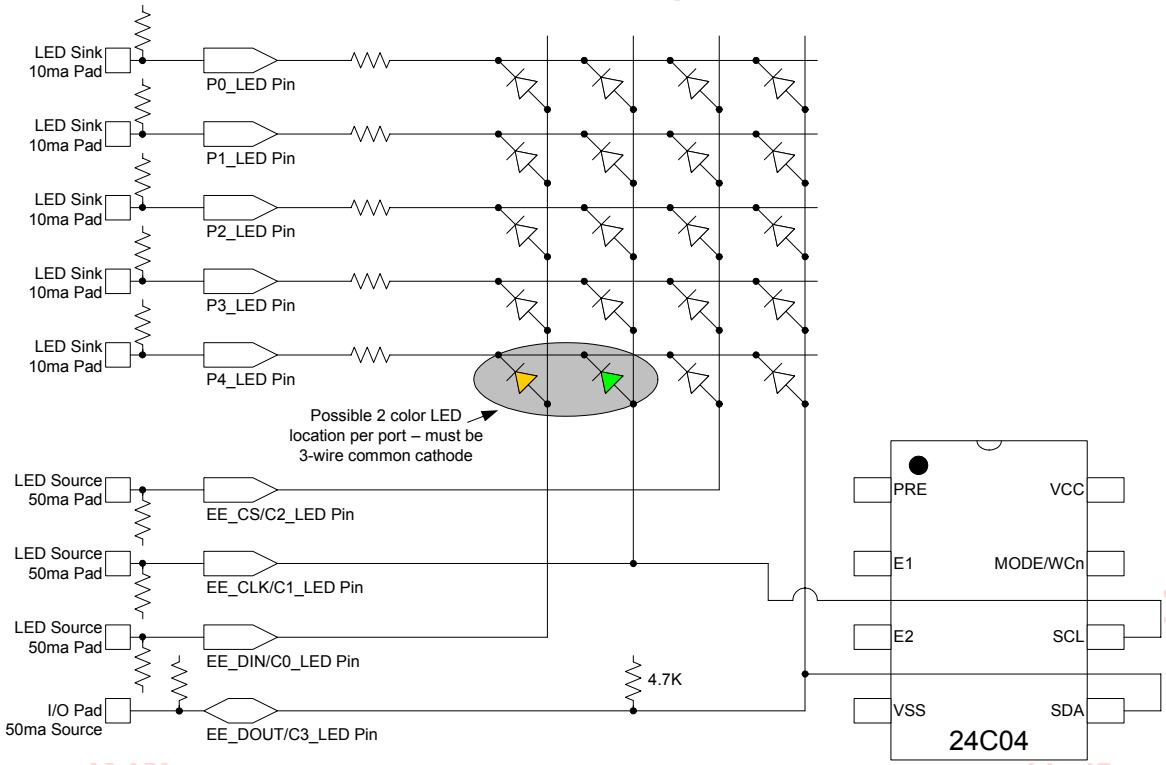


Figure 16: Two LEDs plus 2 wire EEPROM



2.3.1 LED Options

Each port supports up to four LEDs that can be configured individually to show many different options.

These options include:

- Link (off = no link, on = link)
- Activity (off = no activity, on = blink)
- Link/Activity (off = no link, on = link, blink = activity)
- 10 Mbps Link (off = no link, on = 10 Mbps link)
- 10 Mbps Link/Activity (off = no activity, on = 10 Mbps link, blink = activity)
- 100 Mbps Link (off = no link, on = 100 Mbps link)
- 100 Mbps Link/Activity (off = no activity, on = 10 Mbps link, blink = activity)
- 10/100 Mbps Link (off = no link, on = 10/100 Mbps link)
- 10/100 Mbps Link/Activity (off = no activity, on = 10/100 Mbps link, blink = activity)
- Gig Link (off = no link, on = Gig link)
- Gig Link/Activity (off = no activity, on = Gig link, blink = activity)
- 10 Mbps/Gig Link (off = no link, on = 10 Mbps or Gig link)
- 10 Mbps/Gig Link/Activity (off = no activity, on = 10 Mbps or Gig link, blink = activity)
- 100 Mbps/Gig Link (off = no link, on = 100 Mbps or Gig link)
- 100 Mbps/Gig Link/Activity (off = no activity, on = 100 Mbps or Gig link, blink = activity)
- Link/Activity/Speed by blink rate (off = no link, on = link, blink = activity, blink speed = link speed)
- Duplex/Collision (off = half-duplex, on = full-duplex, blink = collision)
- Force Blink
- Force On
- Force Off
- Special (see Section 2.3.2)

Each port's LED options can be configured in the switch port registers (port offset 0x16). Please refer to 88E6350R/88E6350/88E6351 Datasheet Part 2: Switch Core for more information.

2.3.2 Special LEDs

In some applications, two sets of LEDs are desired. One set on the rear panel which would indicate Link/Speed/Activity per port and a second set on the front panel where a common LED can indicate the LAN and/or WAN Activity on a combination of ports. The special LEDs available on the 88E6350R/88E6350/88E6351 device can be used for these types of applications.

Special LEDs are available on Ports 0-3 and can be configured for any of the 4 LEDs available on that port. The special functions are as follows:

Port 0 Special LED – LAN Link/Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Ports 0-4.

Port 1 Special LED – WAN Link Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Port 0.

Port 2 Special LED – Alternate 0 Link/Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable using a bit vector. The default setting shows link/activity on Port 5 (RGMII/GMII port).

Port 3 Special LED – Alternate 1 Link/Activity. This LED can be used to show link and activity on any combination of ports. The ports associated with this LED are user selectable

using a bit vector. The default setting shows link/activity on Port 6 (RGMII/GMII port).

2.3.3 Power up LED Configurations

The power up LED configuration can be set by the LED_SEL[1:0] pins. These pins are internally pulled high, setting a default configuration of 0x3, but can be configured at Reset using 4.7 kohm pull-down resistors.

The functions of each LED for the standard configuration options are given in the following tables:

Table 23: LED_SEL[1:0] = 0x3 (Default)

Port	LED 0 (C0_LED)	LED 1 (C1_LED)	LED 2 (C2_LED)	LED 3 (C3_LED)
Port 0 (P0_LED)	Link/Activity	Gig Link	100/Gig Link	LAN Link/Activity (default for Ports 0-4)
Port 1 (P1_LED)	Link/Activity	Gig Link	100/Gig Link	WAN Link/Activity (default for Port 0)
Port 2 (P2_LED)	Link/Activity	Gig Link	100/Gig Link	Alt Link/Activity (default for Port 5)
Port 3 (P3_LED)	Link/Activity	Gig Link	100/Gig Link	Alt Link/Activity (default for Port 6)
Port 4 (P4_LED)	Link/Activity	Gig Link	100 Gig Link	Reserved

This configuration is designed for systems with one or two LEDs where the first LED can be used to show Link and Activity while the second LED can be used to show a higher speed link has been established (either Gig only or 100/Gig). The special LAN and WAN LEDs can be used on the front panel of the switch to show LAN/WAN activity (see Figure 17).

Figure 17: LED_SEL[1:0] = 0x3 Example Implementation

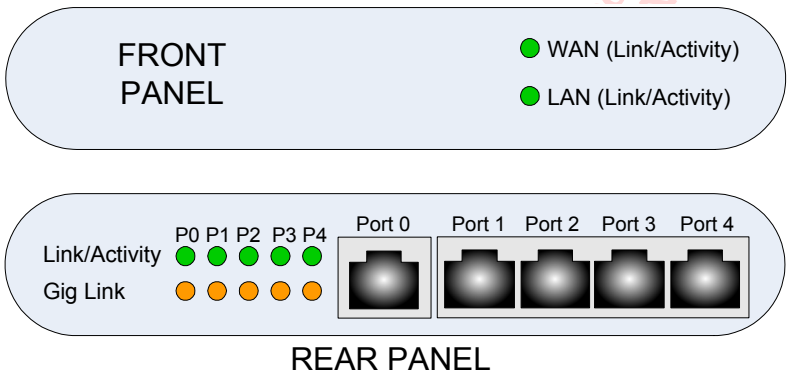


Table 24: LED_SEL[1:0] = 0x2

Port	LED 0 (C0_LED)	LED 1 (C1_LED)	LED 2 (C2_LED)	LED 3 (C3_LED)
Port 0 (P0_LED)	Gig Link/Activity	10/100 Link/Activity	LAN Link/Activity (default for Ports 0-4)	Duplex/Collision
Port 1 (P1_LED)	Gig Link/Activity	10/100 Link/Activity	WAN Link/Activity (default for Port 0)	Duplex/Collision
Port 2 (P2_LED)	Gig Link/Activity	10/100 Link/Activity	Alt Link/Activity (default for Port 5)	Duplex/Collision
Port 3 (P3_LED)	Gig Link/Activity	10/100 Link/Activity	Alt Link/Activity (default for Port 6)	Duplex/Collision
Port 4 (P4_LED)	Gig Link/Activity	10/100 Link/Activity	Reserved	Duplex/Collision

This configuration is designed for systems with two LEDs where one LED is used to show Gig Link and Activity and the second LED is used to show 10/100 Link and Activity. The special LAN and WAN LEDs can be used on the front panel of the switch to show LAN/WAN activity (see Figure 18).

Figure 18: LED_SEL[1:0] = 0x2 Example Implementation

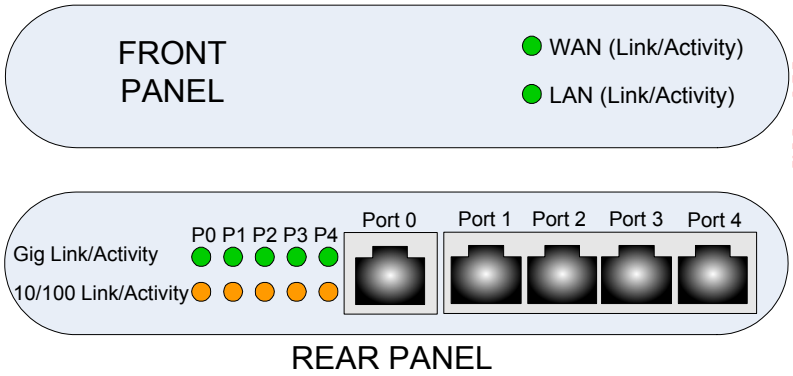


Table 25: LED_SEL[1:0] = 0x1

Port	LED 0 (C0_LED)	LED 1 (C1_LED)	LED 2 (C2_LED)	LED 3 (C3_LED)
Port 0 (P0_LED)	100/Gig Link/Activity	10/100 Link/Activity	10/Gig Link/Activity	Duplex/Collision
Port 1 (P1_LED)	100/Gig Link/Activity	10/100 Link/Activity	10/Gig Link/Activity	Duplex/Collision
Port 2 (P2_LED)	100/Gig Link/Activity	10/100 Link/Activity	10/Gig Link/Activity	Duplex/Collision
Port 3 (P3_LED)	100/Gig Link/Activity	10/100 Link/Activity	10/Gig Link/Activity	Duplex/Collision
Port 4 (P4_LED)	100/Gig Link/Activity	10/100 Link/Activity	10/Gig Link/Activity	Duplex/Collision

This configuration is designed to work with bi-color or tri-color LEDs where one color can be used to show link/activity at one speed, the second color can be used to show link/activity at a second speed, and the third color (or mix of the first two) can be used to show link/activity at the third speed. By using a combination of LED 0, LED 1, and LED 2 the user has the option of using the mixed color to identify any of the three speeds.

If LED 0 and LED 1 are used then the mixed color represents 100 Mbps, if LED0 and LED 2 are used then the mixed color represents Gigabit, and if LED1 and LED2 are used then the mixed color represents 10 Mbps.

For example, if 100 Mbps is to be identified by the mixed color then LED 0 and LED 1 should be used. With this combination, only LED 0 will light if there is Gig Link/Activity and only LED 1 will light if there is 10 Mbps Link/Activity. If there is 100 Mbps Link/Activity then both LED 0 and LED 1 will light causing a mixed color. This example is shown in Figure 19 below.

Figure 19: LED_SEL[1:0] = 0x1 Example Implementation

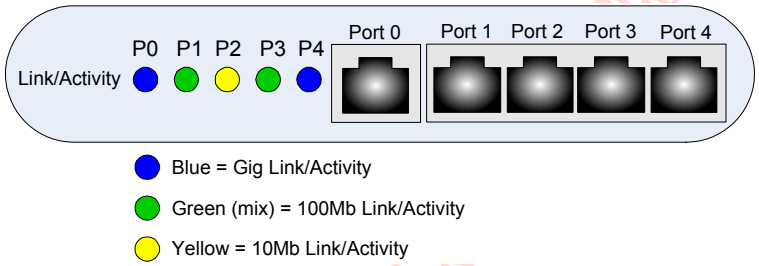
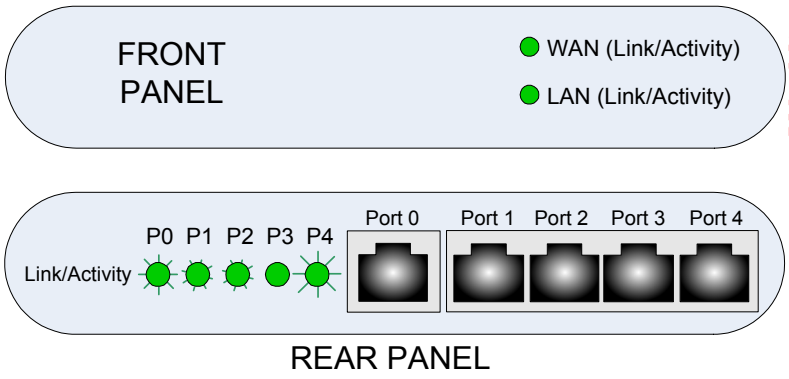


Table 26: LED_SEL[1:0] = 0x0

Port	LED 0 (C0_LED)	LED 1 (C1_LED)	LED 2 (C2_LED)	LED 3 (C3_LED)
Port 0 (P0_LED)	Reserved	Link/Activity/Speed (by blink rate)	Duplex/Collision	LAN Link/Activity (default for Ports 0-4)
Port 1 (P1_LED)	Reserved	Link/Activity/Speed (by blink rate)	Duplex/Collision	WAN Link/Activity (default for Port 0)
Port 2 (P2_LED)	Reserved	Link/Activity/Speed (by blink rate)	Duplex/Collision	Alt Link/Activity (default for Port 5)
Port 3 (P3_LED)	Reserved	Link/Activity/Speed (by blink rate)	Duplex/Collision	Alt Link/Activity (default for Port 6)
Port 4 (P4_LED)	Reserved	Link/Activity/Speed (by blink rate)	Duplex/Collision	Reserved

This configuration is designed for a system with a single LED, where the speed of the link can be observed by the blink rate of the LED (the faster the link, the faster the blink rate). The default blink rates are 84ms for 1 Gbps, 170 ms for 100 Mbps, and 340 ms for 10 Mbps. The special LAN and WAN LEDs can be used on the front panel of the switch to show LAN/WAN activity (see Figure 20).

Figure 20: LED_SEL[1:0] = 0x0 Example Implementation



3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 27: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(3.3)}$	Power Supply Voltage on any 3.3V signal with respect to VSS	-0.5	3.3	+3.6	V
$V_{DD(2.5)}$	Power Supply Voltage on any 2.5V signal with respect to VSS	-0.5	2.5	+3.6 or $V_{DD(3.3)}$ +0.5[1] whichever is less	V
$V_{DD(1.8)}$	Power Supply Voltage on any 1.8V supply with respect to VSS	-0.5	1.8	+3.6 or $V_{DD(2.5)}$ +0.5[2] whichever is less	V
$V_{DD(1.0)}$	Power Supply Voltage on any 1.0V supply with respect to VSS	-0.5	1.0	+3.6 or $V_{DD(1.8)}$ +0.5[3] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to VSS	-0.5		+3.6 or V_{DDO_PIN}[4] +0.5[5] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[6]	°C

1. VDD(2.5) must never be more than 0.5V greater than VDD(3.3) or damage will result. Power must be applied to VDD(3.3) before or at the same time as VDD(2.5).
2. VDD(1.8) must never be more than 0.5V greater than VDD(2.5) or damage will result. Power must be applied to VDD(2.5) before or at the same time as VDD(1.8).
3. VDD(1.0) must never be more than 0.5V greater than VDD(1.8) or damage will result. Power must be applied to VDD(1.8) before or at the same time as VDD(1.0).
4. The VDDO pad ring has separate I/O power supply options. Therefore, the voltage applied to a group of I/O pins must follow what is defined in Section 1.
5. VPIN must never be more than 0.5V greater than VDDO or damage will result.
6. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

3.2 Recommended Operating Conditions

Table 28: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(3.3)}$	3.3V power supply	For any 3.3V supply pin[1]	3.135	3.3	3.465	V
$V_{DD(2.5)}$	2.5V power supply	For any 2.5V supply pin[2]	2.375	2.5	2.625	V
$V_{DD(1.8)}$	1.8V power supply	For any 1.8V supply pin	1.710	1.8	1.890	V
$V_{DD(1.0)}$	1.0V power supply	For any 1.0V supply pin	.950	1.0	1.050	V
T_A	Ambient operating temperature[3]	Commercial parts	0		70	°C
		Industrial parts[4]	-40		85	°C
T_J	Maximum junction temperature				125[2]	°C
RSET	Internal bias reference	External resistor value required to be placed between RSET and VSS pins	4950	5000	5050	Ω

1. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
2. Some VDDO pins can be set to either 1.8V or 2.5V or 3.3V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.375V, and between 2.625V and 3.135V are not supported.
3. The important parameter is maximum junction temperature. As long as the maximum junction temperature is not exceeded, the device can be operated at any ambient temperature. Refer to White Paper on "TJ Thermal Calculations" for more information.
4. Industrial parts have an “I” following the commercial part numbers. See Section 5.1, Ordering Part Numbers and Package Markings, on page 101.

3.3 Thermal Conditions

3.3.1 Thermal Conditions for the 88E6350R device 128-pin TQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 88E6350R device 128-Pin TQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		24.8		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		21.6		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		20.4		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		19.7		°C/W
Ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 88E6350R device 128-Pin TQFP package $\Psi_{JT} = (T_J - T_{TOP})/P$. T_{TOP} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.22		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.33		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.42		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.48		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E6350R device 128-Pin TQFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		7.7		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 88E6350R device 128-Pin TQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		15.5		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.3.2 Thermal Conditions for the 88E6350 device 176-pin TQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 88E6350/88E6351 device 176-Pin TQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		22.1		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		19.3		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		18.4		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		17.9		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 88E6350/88E6351 device 176-Pin TQFP package $\psi_{JT} = (T_J - T_{TOP})/P$. T_{TOP} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.16		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.17		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.19		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.22		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E6350/88E6351 device 176-Pin TQFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		6.6		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 88E6350/88E6351 device 176-Pin TQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		13.7		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.4 Current Consumption

Table 29: 88E6350R/88E6350 Device Current Consumption

Pins	Parameter	Condition	Min	Typ	Max	Units
Px_AVDD	1.8V power to analog core for each Gig PHY interface	All ports active (Port 0 - Port 4 at 1000 Mbps)		529		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		178		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		118		mA
		All ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		529		mA
		All ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		178		mA
		All ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		118		mA
		Reset		7		mA
		No link on any port		32		mA
EE_VDDO	3.3V to EEPROM and LED pins.	All ports active at 1000 Mbps		18		mA
		All ports active at 100 Mbps		10		mA
		All ports active at 10 Mbps		10		mA
		All ports idle and linked at 1000 Mbps		18		mA
		All ports idle and linked at 100 Mbps		10		mA
		All ports idle and linked at 10 Mbps		10		mA
		Reset		15		mA
		No link on any port		2		mA

Table 29: 88E6350R/88E6350 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
VDDO	2.5V to SMI CPU bus and Port 5's and Port 6's GMII/MII I/O pins.	All ports active at 1000 Mbps		58		mA
		All ports active at 100 Mbps		11		mA
		All ports active at 10 Mbps		3		mA
		All ports idle and linked at 1000 Mbps		23		mA
		All ports idle and linked at 100 Mbps		7		mA
		All ports idle and linked at 10 Mbps		1		mA
		Reset		1		mA
		No link on any port		1		mA
	1.8V to SMI CPU bus and Port 5's and Port 6's GMII/MII I/O pins.	All ports active at 1000 Mbps		30		mA
		All ports active at 100 Mbps		6		mA
		All ports active at 10 Mbps		2		mA
		All ports idle and linked at 1000 Mbps		10		mA
		All ports idle and linked at 100 Mbps		2		mA
		All ports idle and linked at 10 Mbps		1		mA
		Reset		1		mA
		No link on any port		1		mA
VDD_ CORE	1.0V power to digital core	All ports active at 1000 Mbps		617		mA
		All ports active at 100 Mbps		210		mA
		All ports active at 10 Mbps		169		mA
		All ports idle and linked at 1000 Mbps		560		mA
		All ports idle and linked at 100 Mbps		205		mA
		All ports idle and linked at 10 Mbps		165		mA
		Reset		30		mA
		No link on any port		121		mA

Table 29: 88E6350R/88E6350 Device Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
AVDD AVDD_PLL	1.8V power common block, PLL block	All ports 1000 Mbps and active		6		mA
		All ports 100 Mbps and active		6		mA
		All ports 10 Mbps and active		6		mA
		All ports 1000 Mbps and idle		6		mA
		All ports 100 Mbps and idle		6		mA
		All ports 10 Mbps and idle		6		mA
		Reset		6		mA
		No link on any port		6		mA
Px_AVDD to V_{CT}	1.8V power common block to External Magnetics Center Tap Pin	All ports active (Port 0 - Port 4 at 1000 Mbps)		512		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		152		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		440		mA
		All ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		512		mA
		All ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		152		mA
		All ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		118		mA
		Reset		4		mA
		No link on any port		7		mA

3.5 DC Electrical Characteristics

3.5.1 Digital Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 30: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	XTAL_IN		1.4		1.99	V
		All others	VDDO = 3.135	2.2			V
			VDDO = 2.375V	1.7			V
			VDDO = 1.710V	1.2			V
V_{IL}	Low level input voltage	XTAL_IN		-0.3		0.54	V
		All others	VDDO = 3.135	-0.4		0.94	V
			VDDO = 2.375V	-0.4		0.7	V
			VDDO = 1.710V	-0.4		0.51	V
V_{OH}	High level output voltage	LED pins	I_{OH} = -8 mA	VDDO - 0.4			V
		All others (except INTn [1])	I_{OH} = -4 mA	VDDO - 0.4			V
V_{OL}	Low level output voltage	INTn and LED pins	I_{OL}= 8 mA			0.4	V
		All others	I_{OL}= 4 mA			0.4	V
I_{ILK}	Input leakage current	With pull-up resistor	$0<V_{IN}<V_{DD}$			+ 10 - 50	µA
		With pull-down resistor	$0<V_{IN}<V_{DD}$			+ 50 - 10	µA
		XTAL_IN - with internal resistor				±80	µA
		All others	$0<V_{IN}<V_{DD}$			±10	µA
C_{IN}	Input capacitance	XTAL_IN			5		pF
		All others				5	pF

1. The INTn is an active low, open drain pin. See INTn description in the Signal Description.

3.6 AC Electrical Specifications

3.6.1 Receiver AC Characteristics

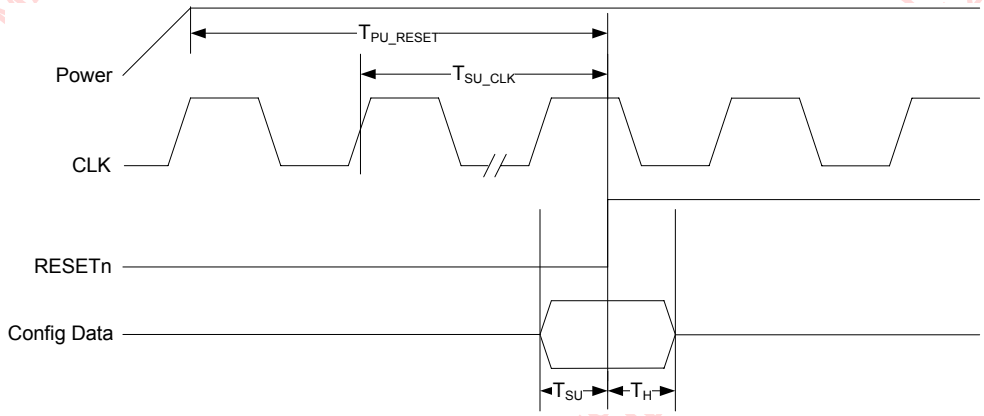
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 31: IEEE DC Transceiver Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted or RESETn assertion time	At power up or sub-sequent resets after power up	10			ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10			Clks
T_{SU}	Configuration data valid prior to RESETn de-asserted[1]		200			ns
T_{HD}	Config data valid after RESETn de-asserted		0			ns

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn. All configuration pins that become outputs during normal operation will remain tri-stated for 40 ns after the rising edge of RESETn.

Figure 21: Reset and Configuration Timing



3.6.2 Clock Timing

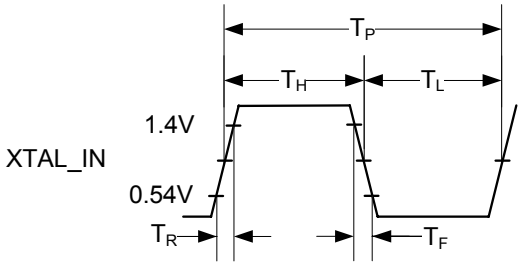
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 32: IEEE DC Transceiver Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns
T_H	XTAL_IN high time		16			ns
T_L	XTAL_IN low time		16			ns
T_R	XTAL_IN rise				3	ns
T_F	XTAL_IN fall				3	ns
$T_{J\_XTAL\_IN}$	XTAL_IN total jitter[2]				200	ps[3]

1. If the crystal option is used, ensure that the frequency is 25.000 MHz ± 50 ppm.
2. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
3. Broadband peak-peak = 200 ps, Broadband rms = 3 ps, 12 kHz to 20 MHz rms = 1 ps.

Figure 22: Oscillator Clock Timing



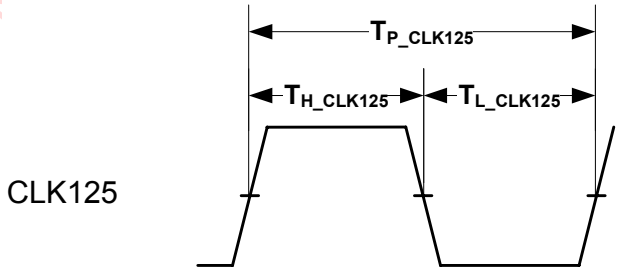
3.6.3 CLK125 Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Table 33: CLK125 Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_CLK125}	CLK125 Period		8 -50 ppm	8	8 +50 ppm	ns
T_{H_CLK125}	CLK125 High time		3.5	4	4.4	ns
T_{L_CLK125}	CLK125 Low time		3.5	4	4.4	ns
T_{J_CLK125}	CLK125 Total Jitter		-	-	80	ps (peak-peak)
T_{P_CD}	CLK125 power up to stable clock delay				300	µs

Figure 23: CLK125 Timing



3.7 GMII Timing

3.7.1 GMII Transmit Timing

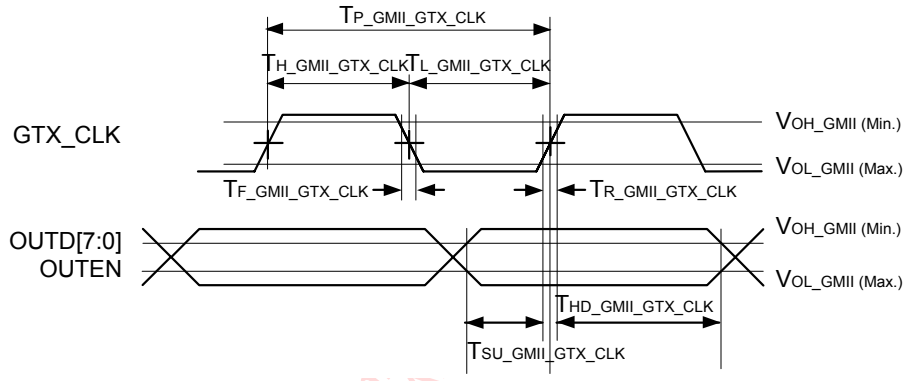
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 34: GMII Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_GTX\_CLK}$	GMII output to clock		2.5			ns
$T_{HD\_GMII\_GTX\_CLK}$	GMII clock to output		0.5			ns
$T_{H\_GMII\_GTX\_CLK}$	GTX_CLK High		2.5[1]		5.5	ns
$T_{L\_GMII\_GTX\_CLK}$	GTX_CLK Low		2.5[1]		5.5	ns
$T_{P\_GMII\_GTX\_CLK}$	GTX_CLK Period		7.5[1]	8.0		ns
$T_{R\_GMII\_GTX\_CLK}$	GTX_CLK Rise Time				1.0	ns
$T_{F\_GMII\_GTX\_CLK}$	GTX_CLK Fall Time				1.0	ns
$T_{RSLEW\_GMII\_GTX\_CLK}$	GTX_CLK Rising Slew Rate		0.6[2]			V/ns
$T_{FSLEW\_GMII\_GTX\_CLK}$	GTX_CLK Falling Slew Rate		0.6[2]			V/ns

1. GTX_CLK numbers not guaranteed during transition between 10/100/1000BASE-T operation.
2. Instantaneous change during internal VIH_GMII (Min.) and VIL_GMII (Max.).

Figure 24: GMII Transmit Timing



3.7.2 GMII Receive Timing

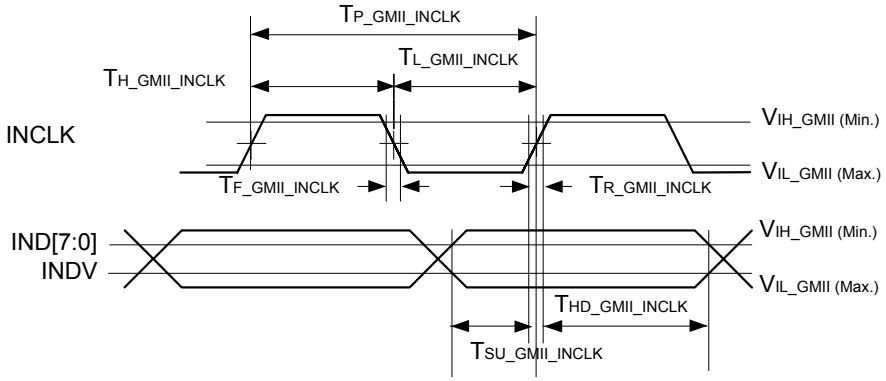
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 35: GMII Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_INCLK}$	GMII Setup Time		2.0			ns
$T_{HD\_GMII\_INCLK}$	GMII Hold Time		0			ns
$T_{H\_GMII\_INCLK}$	INCLK High		2.5[1]			ns
$T_{L\_GMII\_INCLK}$	INCLK Low		2.5[1]			ns
$T_{P\_GMII\_INCLK}$	INCLK Period		7.5[1]	8.0	8.5	ns
F_{GMII_INCLK}	INCLK Frequency		125[1] -100 ppm		125 +100 ppm	MHz
$T_{R\_GMII\_INCLK}$	INCLK Rise Time				1.0	ns
$T_{F\_GMII\_INCLK}$	INCLK Fall Time				1.0	ns

1. RX_CLK toggle rate is “don’t care” if link is down, or if not in 1000BASE-T mode.

Figure 25: GMII Receive Timing



3.8 RGMII Timing

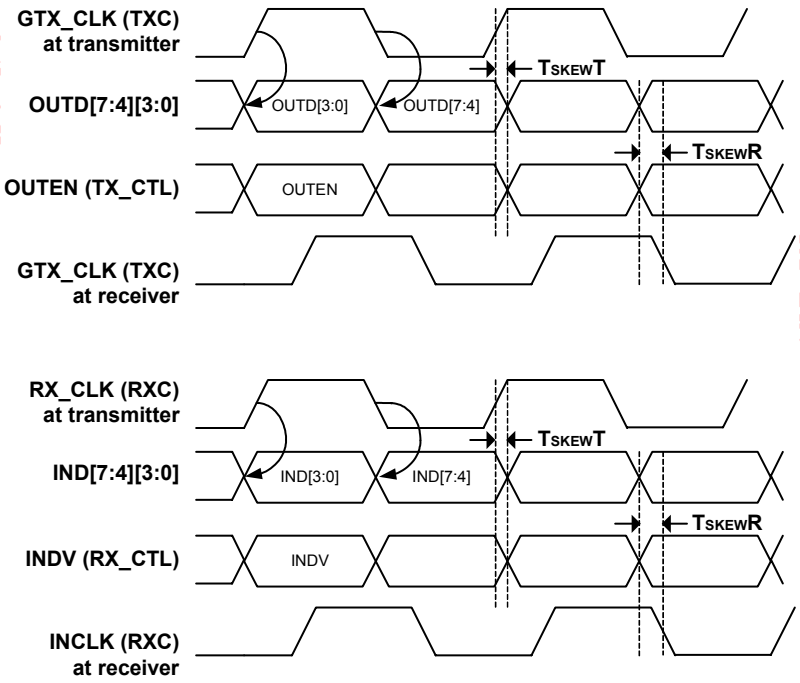
Table 36: RGMII Interface Timing

For other timing modes see Section 3.8.1, RGMII Timing for Different RGMII Modes, on page 85.

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 26: RGMII Multiplexing and Timing



3.8.1 RGMII Timing for Different RGMII Modes

3.8.1.1 RGMII Transmit Timing

Table 37: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{sskew}	RGMII Transmit Delay Control (bit 3) = 0	-0.5		0.5	ns

Figure 27: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (bit 3) = 0

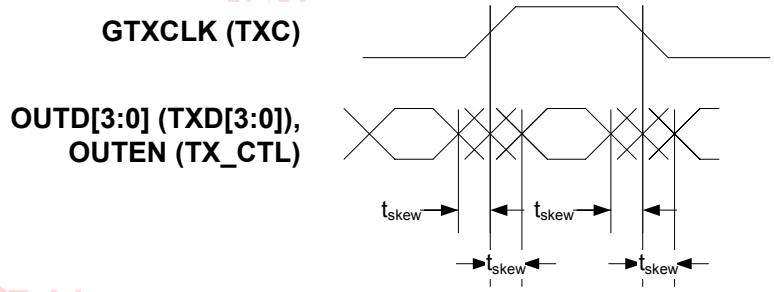
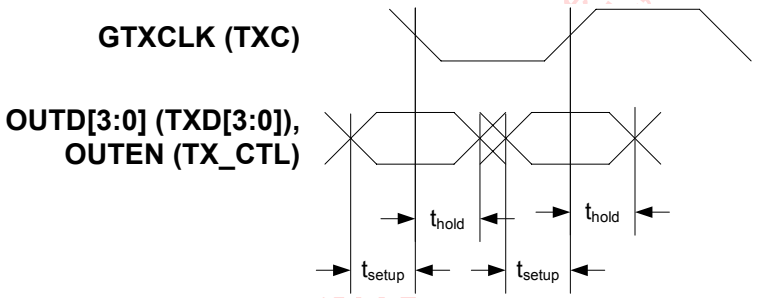


Table 38: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (Offset 0x01, bit 14) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Transmit Delay Control (bit 3) = 1	1.2			ns
t_{hold}		1.0			ns

Figure 28: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (bit 3) = 1



3.8.1.2 RGMII Receive Timing

Table 39: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 0	1.0			ns
t_{hold}		0.8			ns

Figure 29: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0

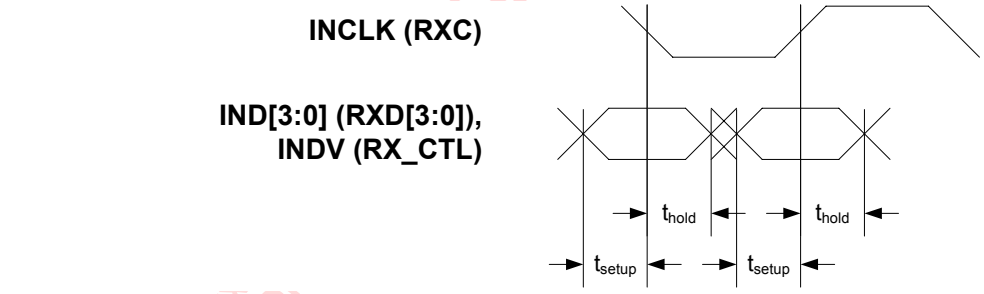
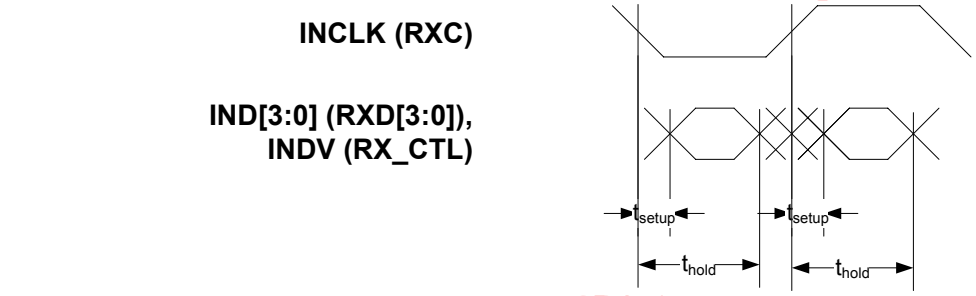


Table 40: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (Offset 0x01, bit 15) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 1	-0.9			ns
t_{hold}		2.7			ns

Figure 30: Receive - RXC Timing when RGMII Receive Delay Control (bit 4) = 1



3.9 MII Timing

3.9.1 MII Clock Timing

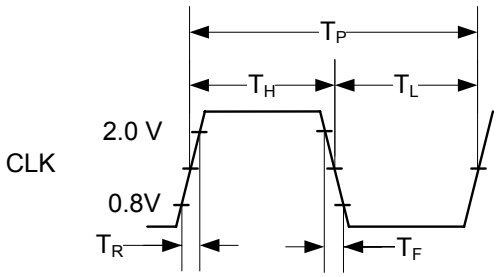
In MII MAC mode, the Px_INCLK and Px_OUTCLK pins are inputs.

Table 41: MII Clock Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	CLK_IN period		20[1]	40 or 400		ns
T_H	CLK_IN high time		8			ns
T_L	CLK_IN low time		8			ns
T_R	CLK_IN rise				3	ns
T_F	CLK_IN fall				3	ns

1. This value applies for 200 Mbps mode

Figure 31: MII Clock Timing



3.9.2 MII Receive Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

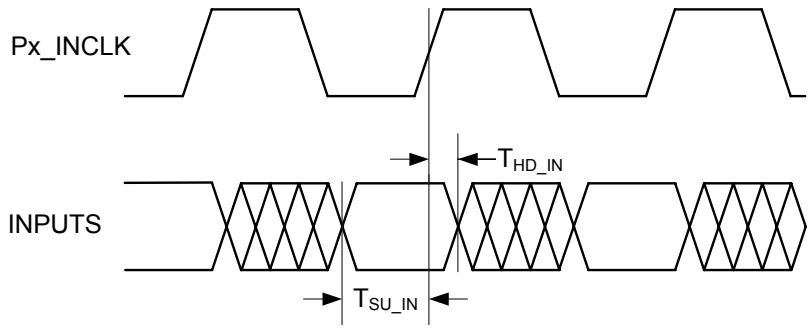
Table 42: MII Receive Timing—100 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid prior to Px_INCLK going high	With 10 pF load	10			ns
T_{HD_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid after Px_INCLK going high	With 10pF load	10			ns

Table 43: MII Receive Timing—200 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid prior to Px_INCLK going high	With 10 pF load	5			ns
T_{HD_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid after Px_INCLK going high	With 10pF load	2			ns

Figure 32: MII Receive Timing



3.9.3 MII Transmit Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 44: MII Transmit Timing—100 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{OUTCLK}	Px_OUTCLK period	10BASE mode[1]		400		ns
		100BASE mode		40		ns
T_{H_OUTCLK}	Px_OUTCLK high	10BASE mode		200		ns
		100BASE mode		20		ns
T_{L_OUTCLK}	Px_OUTCLK low	10BASE mode		200		ns
		100BASE mode		20		ns
T_{CQ_MAX}	Px_OUTCLK to outputs (Px_OUTD[3:0], Px_OUTEN) valid	With 10 pF load			25	ns
T_{CQ_MIN}	Px_OUTCLK to outputs Px_OUTD[3:0], Px_OUTEN) invalid	With 10 pF load	0			ns

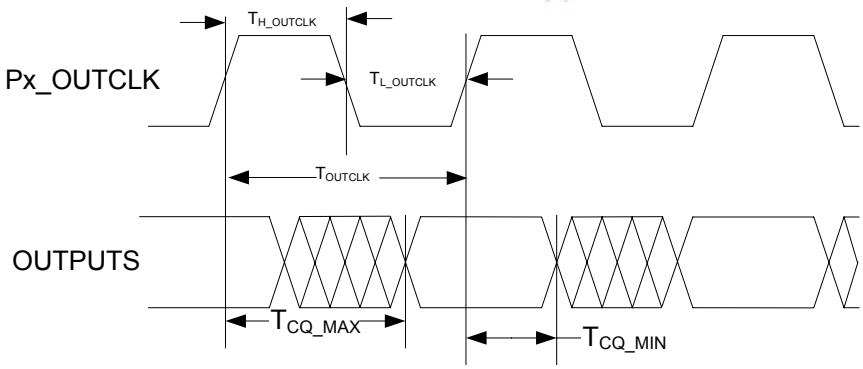
1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps

Table 45: MII Transmit Timing—200 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{OUTCLK}	Px_OUTCLK period	200 Mbps Operation mode[1]		20		ns
T_{H_OUTCLK}	Px_OUTCLK high	200 Mbps Operation		10		ns
T_{L_OUTCLK}	Px_OUTCLK low	200 Mbps Operation		10		ns
T_{CQ_MAX}	Px_OUTCLK to outputs (Px_OUTD[3:0], Px_OUTEN) valid	With 10 pF load			15	ns
T_{CQ_MIN}	Px_OUTCLK to outputs Px_OUTD[3:0], Px_OUTEN) invalid	With 10 pF load	3			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps

Figure 33: MII Transmit Timing



3.10 Serial Management Interface (SMI) Timing

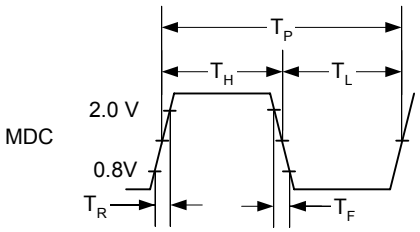
3.10.1 SMI Clock Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 46: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		120			ns	8.33 MHz
T_H	MDC high time		48			ns	
T_L	MDC low time		48			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	

Figure 34: SMI Clock Timing (CPU Set)



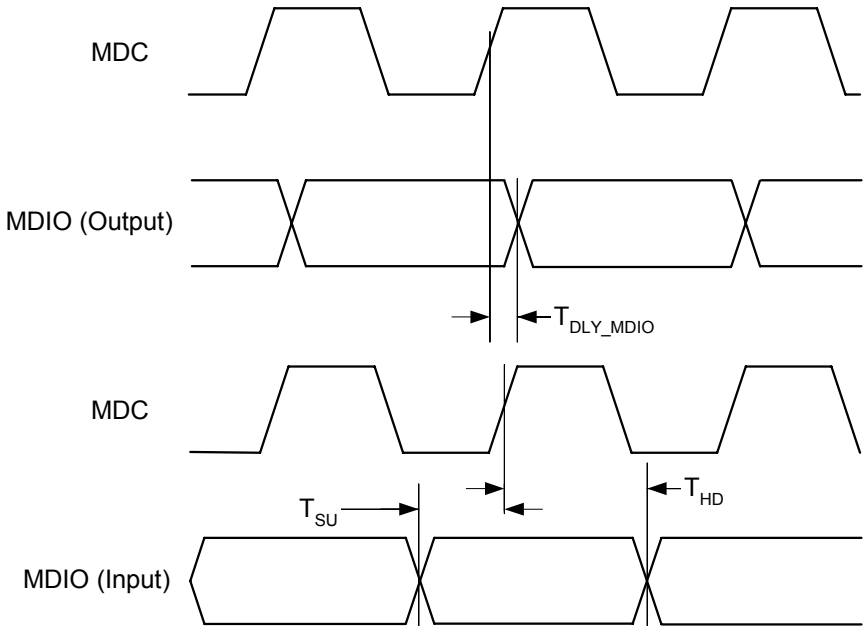
3.10.2 SMI Data Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 47: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		30	ns	
T_{SU}	MDIO (Input) to MDC setup time		10			ns	
T_{HD}	MDIO (Input) to MDC hold time		10			ns	

Figure 35: SMI Data Timing



3.10.3 SMI Timing (PHY Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 48: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		120[1]			ns	8.33 MHz
T_H	MDC high time		48			ns	
T_L	MDC low time		48			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	
T_{TX_SU}	MDIO output setup time		10			ns	2
T_{TX_HD}	MDIO output hold time		10			ns	2
T_{RX_SU}	MDIO input setup time						
T_{RX_HD}	MDIO input hold time						
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		5	ns	3

1. MDC_PHY will track MDC_CPU when the PPU is disabled. When the PPU is enabled the MDC_PHY period will be 240 ns.
2. MDIO input setup and hold time is intentionally sampled with respect to the MDC falling edge.
3. MDIO data is intentionally clocked out on the falling edge of MDC.

Figure 36: SMI Timing Output (PHY Mode)

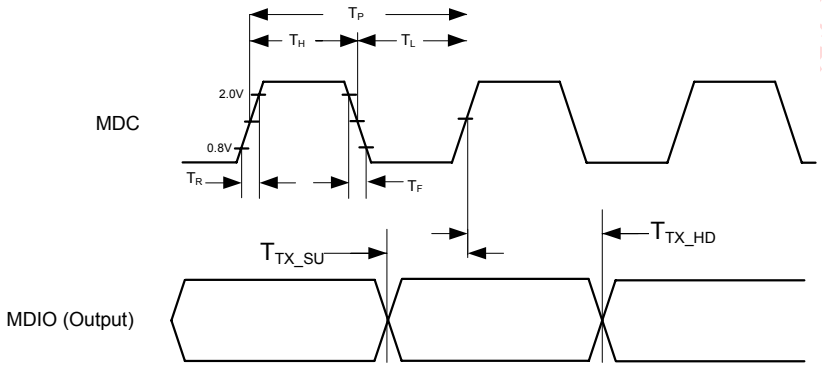
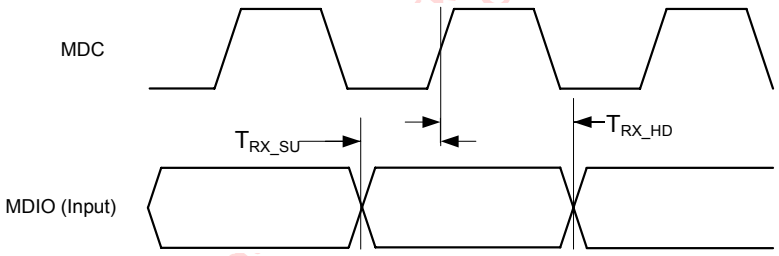


Figure 37: SMI Timing Input (PHY Mode)



3.11 EEPROM Timing

3.11.1 2-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 49: 2-Wire EEPROM Input Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			20000		ns
T_H	EE_CLK high time			10000		ns
T_L	EE_CLK low time			10000		ns
T_{IN}	EE_CLK input time		50		5000	ns

Figure 38: 2-Wire Input Timing

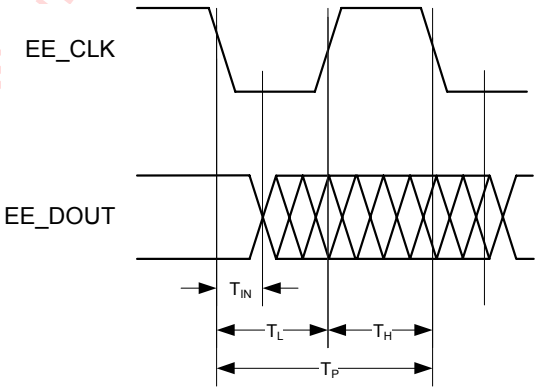
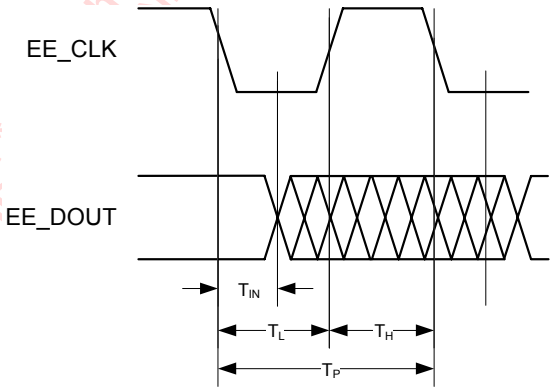


Table 50: 2-Wire EEPROM Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			20000		ns
T_H	EE_CLK high time			10000		ns
T_L	EE_CLK low time			10000		ns
T_{IN}	EE_CLK output time		0		10000	ns

Figure 39: 2-Wire Output Timing



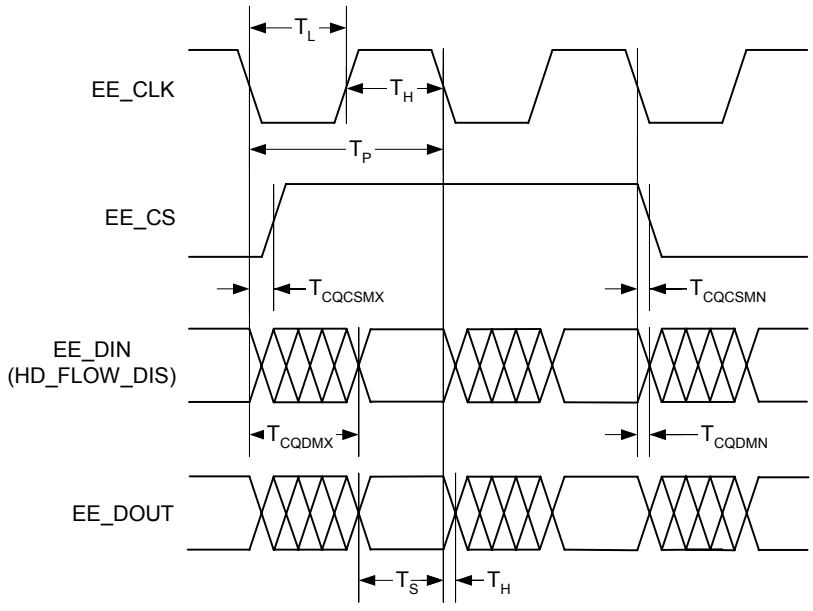
3.11.2 4-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 51: 4-Wire EEPROM Timing

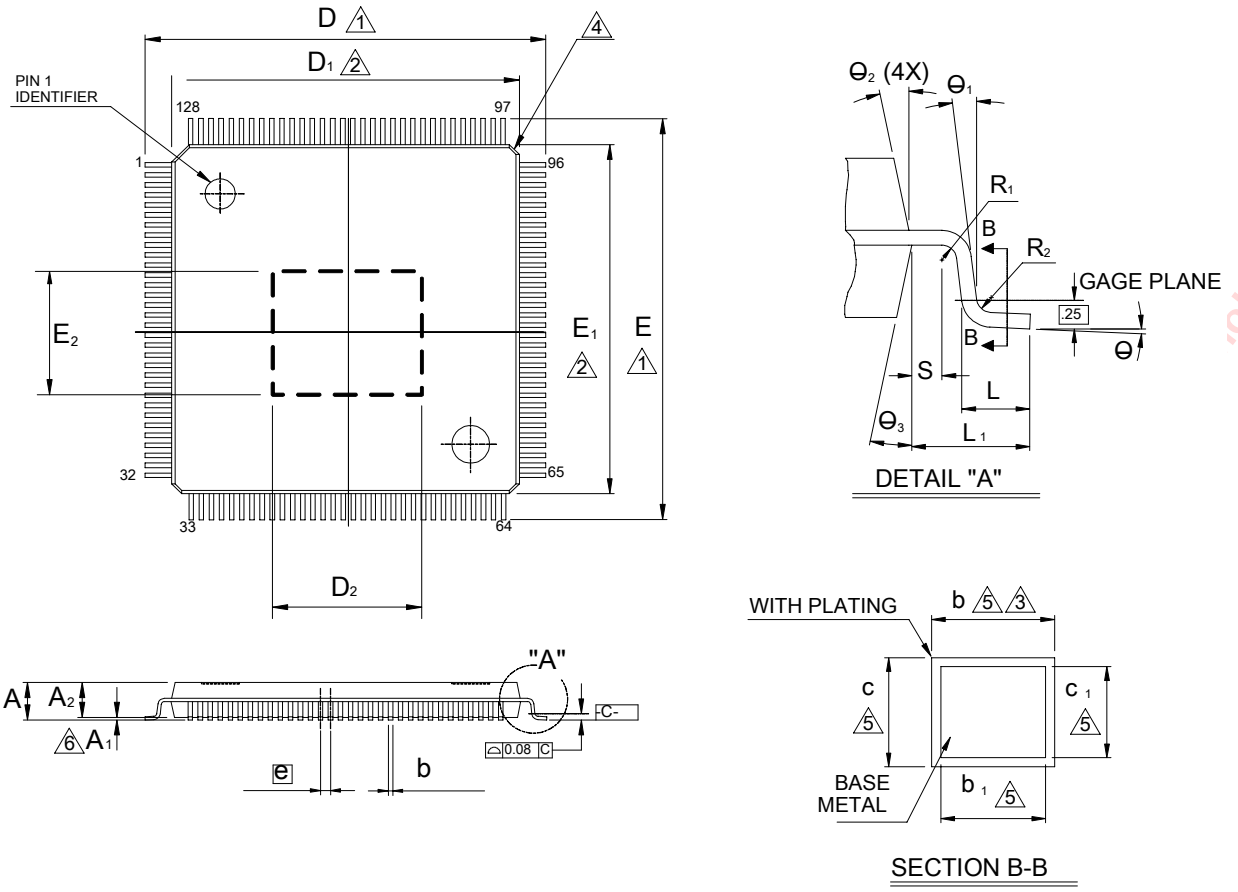
Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			10000		ns
T_H	EE_CLK high time			5000		ns
T_L	EE_CLK low time			5000		ns
T_{CQCSMX}	Serial EEPROM chip select valid	Referenced to EE_CLK			5	ns
T_{CQCSMN}	Serial EEPROM chip select invalid				5	ns
T_{CQDMX}	Serial EEPROM data transmitted to EEPROM valid				10	ns
T_{CQDMN}	Serial EEPROM data transmitted to EEPROM invalid		0			ns
T_S	Setup time for data received from EEPROM		10			ns
T_H	Hold time for data received from EEPROM		10			ns

Figure 40: 4-Wire EEPROM Timing



4 Package Mechanical Dimensions

Figure 41: 88E6350R 128-pin TQFP EPAD Package Mechanical Drawings



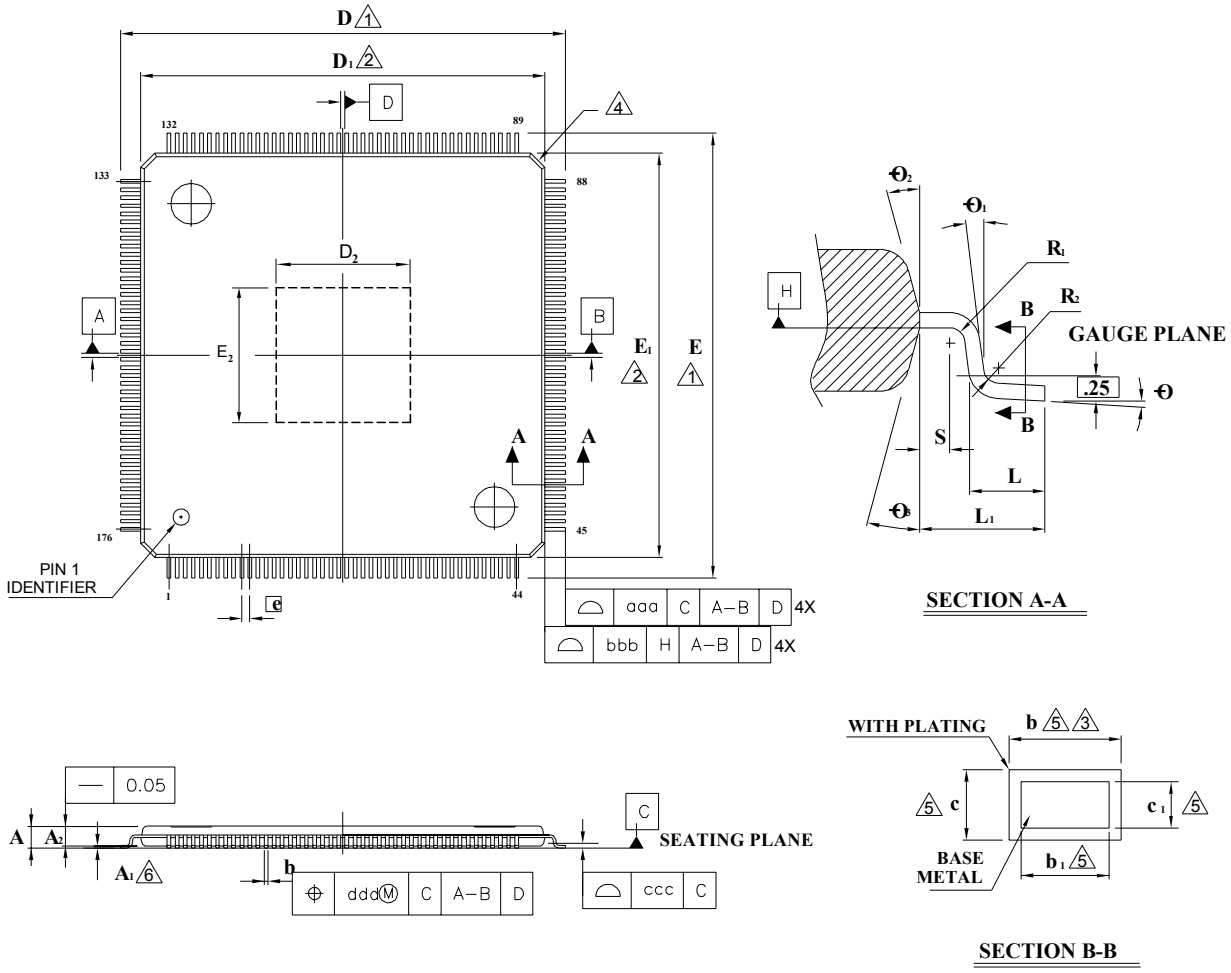
NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Table 52: 88E6350R 128-pin TQFP EPAD Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	--	--	1.20
A_1	0.05	--	0.15
A_2	0.95	1.00	1.05
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	--	0.20
c_1	0.09	--	0.16
D	16.00 BSC		
D_1	14.00 BSC		
E	16.00 BSC		
E_1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	--	--
R_2	0.08	--	0.20
S	0.20	--	--
D_2	6.29 BSC		
E_2	5.41 BSC		
θ	0°	3.5°	7°
θ_1	0°	--	--
θ_2	11°	12°	13°
θ_3	11°	12°	13°

Figure 42: 88E6350/88E6351 176-pin TQFP EPAD Package Mechanical Drawings



NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
   INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD
   BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE
   TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Table 53: 88E6350/88E6351 176-pin TQFP EPAD Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	1.00	1.10	1.20
A_1	0.05	0.10	0.15
A_2	0.95	1.00	1.05
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	--	0.20
c_1	0.09	--	0.16
D	22.00 BSC		
D_1	20.00 BSC		
E	22.00 BSC		
E_1	20.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	--	--
R_2	0.08	--	0.20
S	0.20	--	--
D_2	5.79		
E_2	5.79		
θ	0°	3.5°	7°
θ_1	0°	--	--
θ_2	11°	12°	13°
θ_3	11°	12°	13°
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.07		

5 Ordering Information

5.1 Ordering Part Numbers and Package Markings

Figure 43 shows the ordering part numbering scheme for the devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 43: Sample Part Number

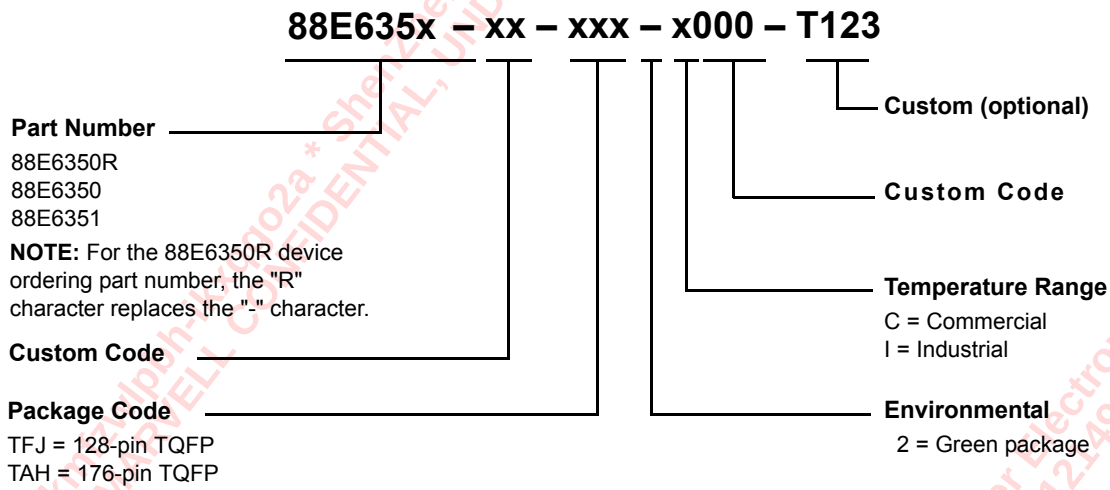


Table 54: 88E6350R/88E6350/88E6351 Commercial Part Order Options

Package Type	Part Order Number
88E6350R 128-pin TQFP	88E6350Rxx-TFJ2C000
88E6350 176-pin TQFP	88E6350-xx-TAH2C000
88E6351 176-pin TQFP	88E6351-xx-TAH2C000

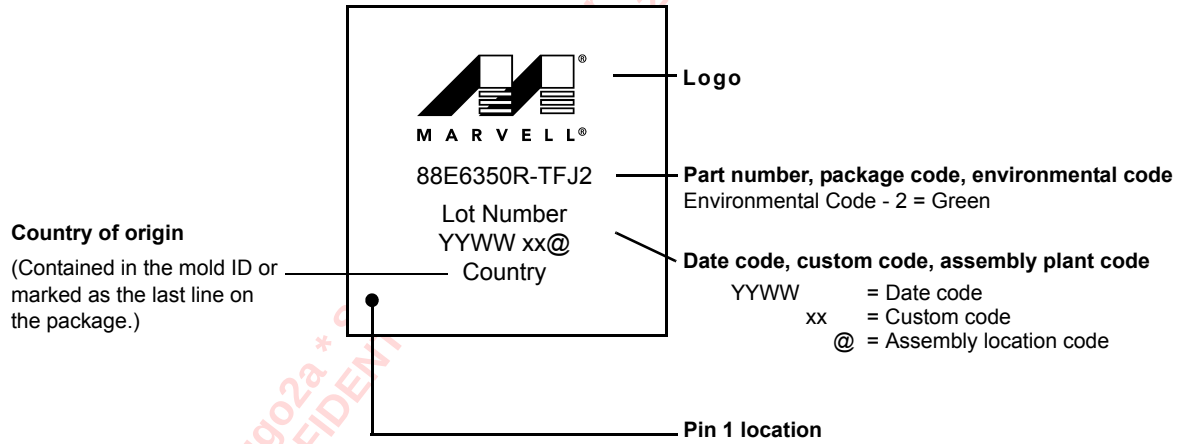
Table 55: 88E6350R/88E6350/88E6351 Industrial Part Order Options

Package Type	Part Order Number
88E6350R 128-pin TQFP	88E6350Rxx-TFJ2I000
88E6351 176-pin TQFP	88E6351-xx-TAH2I000

5.1.1 Commercial Marking Examples

Figure 44 is an example of the package marking and pin 1 location for the 88E6350R 128-pin TQFP Green compliant package.

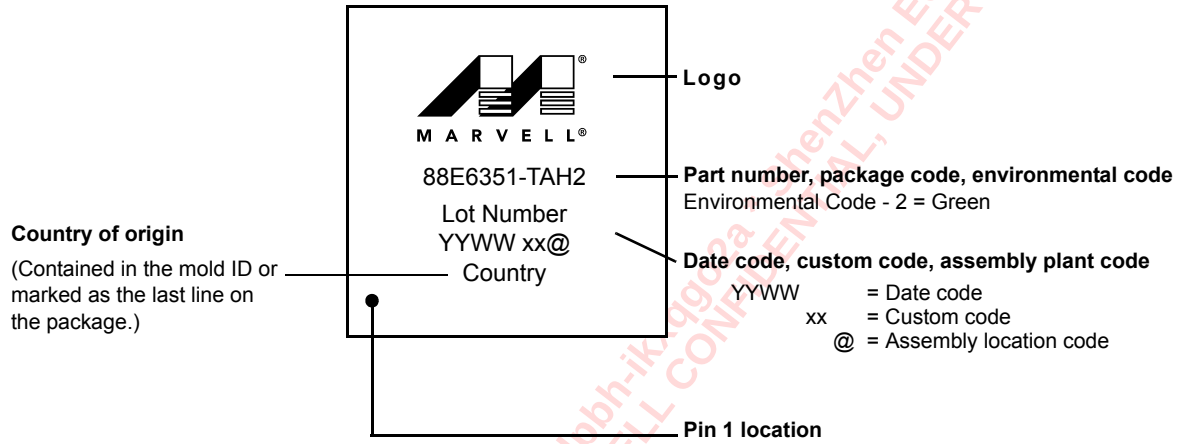
Figure 44: 88E6350R 128-pin TQFP Commercial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 45 is an example of the package marking and pin 1 location for the 88E6351 176-pin TQFP Green compliant package.

Figure 45: 88E6351 176-pin TQFP Commercial Green Compliant Package Marking and Pin 1 Location

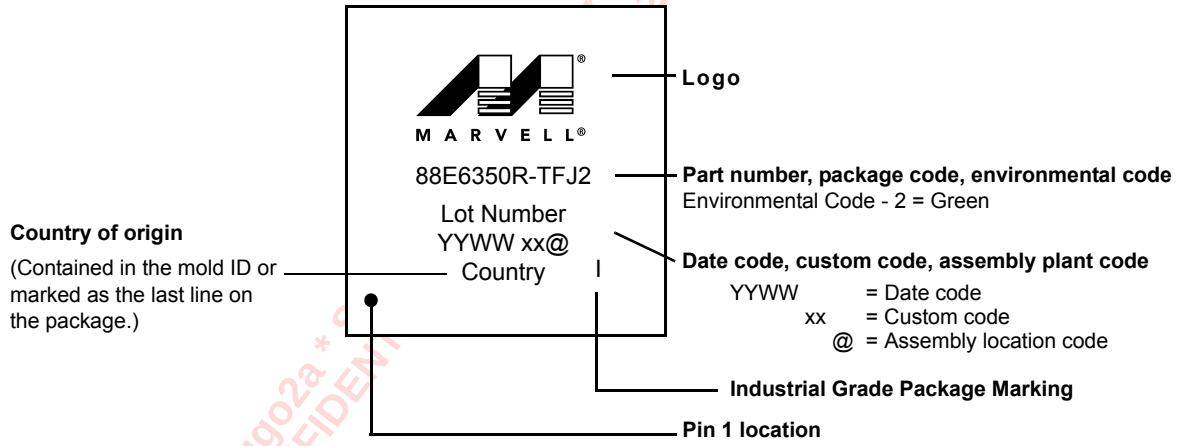


Note: The above example is not drawn to scale. Location of markings is approximate.

5.1.2 Industrial Marking Examples

Figure 46 is an example of the package marking and pin 1 location for the 88E6350R 128-pin TQFP Green compliant package.

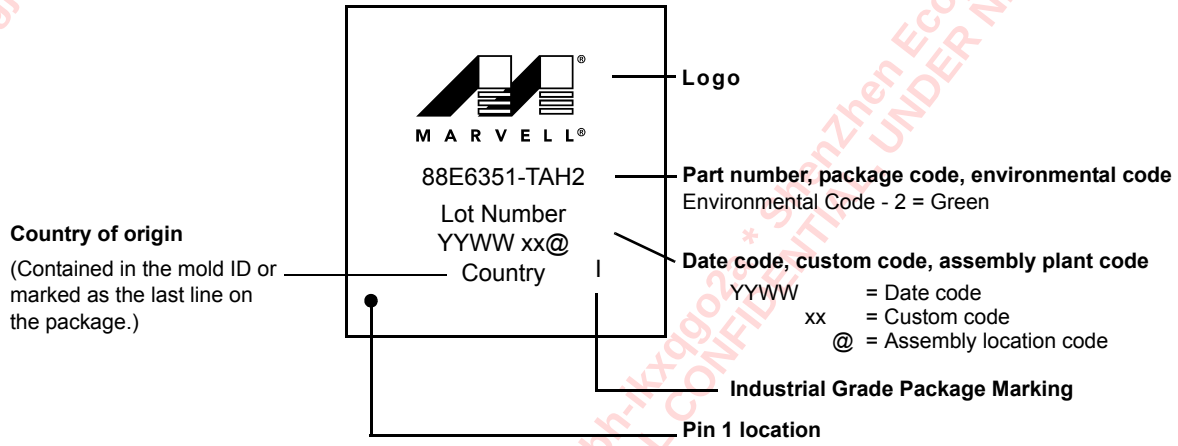
Figure 46: 88E6350R 128-pin TQFP Industrial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 47 is an example of the package marking and pin 1 location for the 88E6351 176-pin TQFP Green compliant package.

Figure 47: 88E6351 176-pin TQFP Industrial Green Compliant Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

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